Eleventh Pacific Northwest Test Workshop
aka: BAST 2002
Bodega Bay, California, Feb 5 - 8, 2002
CALL FOR PARTICIPATION

Committee:
- General Chair: E.J. McCluskey, Stanford
- Vice-General Chair: R. Chandramouli, Synopsys
- Assistant General Chair: Subhasish Mitra, Intel
- Program Chair: Scott Davidson, Sun
- Registration Chair: James Li, Stanford
- Local Arrangements: Mike Purtell, Advantest
- Publicity Chair: Mike Purtell, Advantest
- Finance Chair/IEEE Liaison: Sungorh Yoon, Stanford
- Entertainment Chair: Davia Lu, IBM
- Steering Committee: E.J. McCluskey, Stanford
  R. Chandramouli, Synopsys
  Siyad Ma, Zettacom
  Mike Purtell, Advantest
- Program Committee: Scott Davidson (Chair)
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  Bulent Dervisoglu, Cadence
  Hong Hao, LSI Logic
  Kee Sup Kim, Intel
  Eric Larson, Teradyne
  Zhi-Min Ling, Xilinx
  Samy Makar, Transmeta
  Mike Purtell, Advantest
  John Waicukauski, Synopsys
  Burnell West, Schlumberger

The 11th annual BAST workshop, co-sponsored by the Stanford University Center for Reliable Computing (CRC) and the IEEE Computer Society Test Technology Technical Council (TTTC)*, will be held February 5 - 8, 2002, in Bodega Bay, California. BAST is an informal workshop whose objective is to bring together engineers from the Pacific Northwest to discuss current work on testing electronic circuits.

Attendance at BAST is restricted to fewer than 50 persons in order to facilitate better sharing of ideas. This workshop is unique in that all attendees are on the program; everyone attending is expected to stay at the workshop for its duration, and to participate. Interaction is encouraged during every presentation, and during breaks and social events. Programs and reports from previous BAST workshops are available from the web site listed at the bottom of this page.

Interested persons are invited to submit a proposal containing a brief abstract of what they would like to present. Possible suggestions include:

- System on Chip Test Methodology
- Mixed Signal Testing
- Impact of Deep Sub-micron Test on ATE
- Verification
- Design for Debug and Testability
- Embedded Memory Test
- Fault Coverage and Fault Models
- Future Test Issues
- Test Research
- Testing High Speed Designs
- Online Test

This is not an exclusive list; all interesting abstracts related to test are invited for submission (see reverse side for application information). If you are interested in attending, please email a softcopy of your proposal immediately to:

James Li
E-mail: cmli@crc.stanford.edu
Gates Bldg. 2A, Room 238
Voice: 650-725-0488
Stanford, CA 94305
FAX: 650-723-1451

Applications to attend the workshop will be considered on a first come first serve basis. Your proposal submission will reserve you a place and is not considered a commitment. **Invitations will be mailed out promptly upon receipt of your proposal.** There is no on-site registration.

Bast web site: [http://crc.stanford.edu/BAST/BAST.html](http://crc.stanford.edu/BAST/BAST.html)

* Approval Pending
Proposal for Participation, Please turn in immediately.

Name:_______________________________________________
Address:_____________________________________________

____________________________________________________
Tel.: (       ) _______________ Fax: (       ) _______________
E-Mail:______________________________________________
Company or University: __________________________________

ATTENDEE INFORMATION

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Abstract of your discussion: (Please be brief)