BAST ‘98 Workshop Program

The Inn at the Tides, Bodega Bay, California
February 10-13, 1998

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Tuesday, Feb 10

6:30 PM - 7:30 PM  Registration & Reception

7:30 PM  Dinner & Remarks: Solomon W. Golomb, Univ. of Southern California
BAST ‘98 Workshop Program

Wednesday, Feb 11

7:15 AM  
CONTINENTAL BREAKFAST

8:15 AM - 8:20 AM  
Welcome  
E. J. McCluskey, General Chairman

8:20 AM - 8:25 AM  
Introduction  
R. Chandramouli, Program Chairman

8:30 AM - 9:30 AM  
Session 1  
Testing Core-based Designs  
Session Chair: E. J. McCluskey, CRC, Stanford University

1.1  Recent Experience in Designing Systems Chips, Chit Mallipedi, Cadence
1.2  IP-Based Test Methodology, Sobhan Mukherji, Fujitsu
1.3  A Structured Test Methodology for Systems on Silicon, Sandeep Bhatia, Duet Technologies
1.4  Firing Line: Huong Nguyen, LSI Logic, Wern Yan-Koe, NEC

9:30 AM - 10:30 AM  
BREAK

10:30 AM - 11:30 AM  
Session 2  
ATPG For Next Generation Designs  
Session Chair: R. Chandramouli, Synopsys

2.1  Next Generation ATPG, John Waicukauski, Synopsys
2.2  Behavior ATPG: Is It Time Yet? Manzer Masud, TSSI
2.3  Applying Academic ATPG and Simulation Tools to Real Industrial Circuits, Jon Colburn, UC Santa Cruz
2.4  Firing Line: Tracy Larrabee, UC Santa Cruz, Carol Tong, Synopsys

12:00 PM - 1:00 PM  
LUNCH at Poolside (weather permitting)

1:30 PM - 2:30 PM  
Session 3  
Can ATEs Handle Next Generation Designs?  
Session Chair: Richard Swan, Tuross Corporation

3.1  Next Generation Test Challenges, Mike Purtell, Advantest
3.2  Next Generation Test Description Languages, Tony Taylor, TSSI
3.3  Practical Integration of ATE and Heuristic Fault Location, Bruce Parnas, Advantest America
3.4  Firing Line: Kevin Giebel, Teradyne STD, Scott Keller, LSI Logic

2:30 PM - 3:30 PM  
BREAK

3:30 PM - 4:30 PM  
Session 4  
Can Diagnosis Cope With Newer Technologies?  
Session Chair: Mike Purtell, Advantest

4.1  Diagnosing Digital/Analog/RF Prototypes, Davia Lu, IBM
4.2  Is a FIB a Lie? Creating and Validating Practical Logic Diagnosis Software, Brian Chess, Hewlett-Packard
4.3  Diagnosing Bridging Faults in Industrial Circuits: Theory and Experiment Design, David Lavo, UC Santa Cruz
4.4  Firing Line: Hong Hao, NeoParadigm, Xiaooing Wen, Syntest Technologies

6:00 PM  
DINNER

8:00 PM  
FUN & GAMES

The Inn at the Tides, Bodega Bay, CA  
February 10-13, 1998
Thursday, Feb 12

7:30 AM
CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM
Session 5  Glimpses Into Mixed-Signal Test
Session Chair:  Nirmal Saxena, CRC, Stanford University

5.1 New Approaches for Mixed Signal Test, Bozena Kaminska, OpMaxx
5.2 Defect Based Testing and Yield Improvement, Manuel A. d’Abreu, Level One Communication
5.3 Problems in Testing Analog and Mixed Signal Core, Hong Hao, NeoParadigm Labs
5.4 Firing Line: Stan Cram, National Semiconductor, Leon Sassoon, Level One Communication

9:30 AM - 10:30 AM
BREAK

10:30 AM-11:30 AM
Session 6  Error Correcting Codes And Fault Tolerance
Session Chair:  Siyad Ma, AMD

6.1 Synthesis of Error Correction and Detection Logic, Nirmal Saxena, CRC, Stanford University
6.2 Fault Tolerance in a Space Environment, Philip P. Shirvani, CRC, Stanford University
6.3 Algorithm Based Fault-Tolerance, Robert Redinbo, UC Davis
6.4 Firing Line: Bruce Parnas, Advantest America, Yervent Zorian, Logic Vision

12:00 PM - 1:00 PM
LUNCH
at Poolside (weather permitting)

AFTERNOON: INDIVIDUAL DISCUSSION

7:30 PM - 9:30 PM
PANEL DISCUSSION
at Bay View Room

Creature From Blue Lagoon: 50M Transistors, 3K I/O, Digital, Analog, Mixed-Signal, Programmable Cores (soft, hard) from Multiple Vendors, GigaHertz Clock Rates and Low Power;
Can We Test This Monster?

Moderator:  E. J. McCluskey, CRC, Stanford University
Panelist:  Hisahige Ando, HAL Computers
          Hong Hao, NeoParadigm Labs
          Scott Keller, LSI Logic
          Shigeru Sugamori, Advantest
          Richard Swan, Tuross Corporation
          Yervent Zorian, LogicVision
FRIDAY, FEB 13

7:30 AM
CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM
Session 7    Advances In Fault Modeling
Session Chair: Tracy Larrabee, UC Santa Cruz

7.1 Deep Fault — A New Paradigm for ATPG, Scott Davidson, Sun Microsystems
7.2 Encoding Techniques for Delay Fault Testability, Subhasish Mitra, CRC, Stanford University
7.3 Fault Coverage Discrepancies Among Various ATPG Tools, London Jin, Adaptec
7.4 Firing Line: Bechir Ayari, Duet Technologies, Alex Miczo, Cypress Semiconductor

9:30 AM - 10:30 AM
BREAT

CHECKOUT (before noon)

10:30 AM-11:30 AM
Session 8    Are All Test Methodologies The Same?
Session Chair: Davia Lu, IBM

8.1 A Comparison of Bridging Fault Simulation Methods, Scott Fetherston, AMD
8.2 Test Chip Experiment — Experimental Results from the Final Package Test, Jonathan T. Y. Chang, CRC, Stanford University
8.3 High Speed Microprocessor Test Challenges, David M. Wu, Intel
8.4 Firing Line: Joel Ferguson, UC Santa Cruz, Samy Makar, Cirrus Logic

11:30 AM - 12:00 Noon
Closing Remarks
Questionnaire Collection

12:30 PM - 1:30 PM
LUNCH
at Poolside (weather permitting)