BAST ’99 Workshop Program

The Inn at the Tides, Bodega Bay, California
February 23-26, 1999

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BAST ’99 Workshop Program

*** Tuesday, Feb 23 ***

6:30 PM - 7:30 PM Registration & Reception
7:30 PM - 8:30 PM Dinner
8:30 PM - 9:00 PM Remarks: Prof. John McCarthy, Stanford University

*** Wednesday, Feb 24 ***

7:15 AM CONTINENTAL BREAKFAST
8:15 AM - 8:20 AM Welcome E. J. McCluskey, General Chairman
8:20 AM - 8:25 AM Introduction Siyad Ma, Program Chairman
8:30 AM - 9:30 AM Session 1 Comparing Test Techniques

Session Chair: Edward J. McCluskey, Stanford CRC
1.1 A Technique for Comparing Test Methods, Rohit Kapur, Synopsys
1.2 Experimental Results on Test Techniques, Kan-Yuan Cheng, Stanford CRC
1.3 A Comparison of Bridging Fault Simulation Methods, Siyad Ma, AMD
1.4 Firing Line: John Waiccuauski, Synopsys, Philip Shirvani, Stanford CRC

9:30 AM - 10:30 AM BREAK

10:30 AM - 11:30 AM Session 2 Testing Next Generation Design

Session Chair: Robert Redinbo, UC Davis
2.1 Challenges of Embedded Memory Test in 21st Century, Mike Lin, Intel
2.2 Making a Cell Library More Testable: A Case Study Using Cyrix's 0.18um Standard Cell Library, Rahul Kundu, UC Santa Cruz
2.3 Design & Test of Mixed-Signal ICs - Current and Future Challenges, Manuel d'Abreu, Level One Comm.
2.4 Firing Line: Jacob Abraham, UT Austin & Stanford CRC, Brian Chess, HP

12:00 PM - 1:00 PM LUNCH

1:30 PM - 2:30 PM Session 3 Analog and Mixed-Signal Test

Session Chair: Marc Levitt, Sonics Inc.
3.1 Parametric Faults Coverage of Analog Circuits in Low Voltage Testing Methodology, Chao-Wen Tseng, Stanford CRC
3.2 Low Voltage testing of PLL, James Li, Stanford CRC
3.3 Testing High Resolution A/D Converters, Derek Floyd, HP
3.4 Firing Line: Jose Santiago, VLSI Technology, Davia Lu, IBM

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2:30 PM - 3:30 PM  
BREAK

3:30 PM - 4:30 PM  
**Session 4  Tester Issues**
Session Chair: Davia Lu, IBM

4.1 Mixed Signal Test on VLSI testers, *Eric Larson, Teradyne*

4.2 Reducing Test Escapes for Gigabit Rage Devices in a 5 Second Test,  
*Dennis Petrich, Wavecrest*

4.3 Low Cost Testers - Not Trailing Edge Technology, *Garry Gillette, Credence*

4.4 Firing Line: *Fred Watt, Finley Design, Mike Purcell, Advantest*

7:00 PM  
DINNER

8:00 PM  
FUN & GAMES
Thursday, Feb 25

7:30 AM
CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM
Session 5  Test Software
Session Chair:  Bob Huston, Credence

5.1 Virtual Test, Tom Austin, Teradyne
5.2 Some issues in vector translation, Bruce Parnas, Advantest
5.3 What is Next in ATE Software? Hira Ranga, Credence
5.4 Firing Line:  Bill Bottoms, Credence, Bill Chown, IMS

9:30 AM - 10:30 AM
BREAK

10:30 AM-11:30 AM
Session 6  Distributed Test
Session Chair:  Mike Purtell, Advantest

6.1 Partitioned Test and Synthesized ATE, Marc Loranger, Credence
6.2 Distributed Testing - Meeting Challenges of DSM, Mike Kondrat, Opmaxx
6.3 Does BOST make sense? Kevin Giebel, Teradyne
6.4 Firing Line:  Bruce Parnas, Advantest, Givargis Danialy, LogicVision

12:00 PM - 1:00 PM
LUNCH

AFTERNOON FREE
7:30 PM - 9:30 PM

PANEL DISCUSSION

at Bay View Room

Proposed Panel: Test Wisdom from the Veterans

Panel Chair: E. J. McCluskey, CRC, Stanford University
Panelist: John Waicukauski, Synopsys
Peggy Nissen, AMD
Bob Huston, Credence
Bill Bottoms, Credence
Friday, Feb 26

7:30 AM  
CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM  
**Session 7  System-On-a-Chip Test**  
Session Chair: Jacob Abraham, Stanford CRC & UT Austin

7.1 Design Considerations in Developing and Integrating Analog/Mixed-Signal in Systems-on-a-Chip, *Henry Chang, Cadence*

7.2 Handling Multiple Clocks in Scan Design, *Samy Makar, Cirrus Logic*

7.3 System-on-Chip Debug and Test, *Marc Levitt, Sonics Inc.*

7.4 Firing Line: *Peggy Nissen, AMD, Robert Redinbo, UC Davis*

9:30 AM - 10:30 AM  
BREAK

**CHECKOUT (before 11:00am)**

10:30 AM-11:30 AM  
**Session 8  Test Generation Beyond Stuck-At Faults**  
Session Chair: Siyad Ma, AMD

8.1 Test Generation for Delay Faults, *Jacob Abraham, Stanford CRC & UT Austin*

8.2 Why Two Fault Models Should Be Used for IDDQ, *Bob Duell, Synopsys*

8.3 Efficient Modeling and ATPG for Embedded RAMs in a Near Full-Scan Circuit, *John Waicukauski, Synopsys*

8.4 Firing Line: *Marly Rocken, Intel, Manzer Masud, TSSI*

11:30 AM - 12:00 Noon  
Closing Remarks  
Questionnaire Collection

12:30 PM - 1:30 PM  
LUNCH  
*at Poolside (weather permitting)*