



## FPGA Interconnect Delay Fault Testing

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## Proposed Testing Method Characteristics

- Test routing resources
  - 80% of FPGA is routing resources
- High fault coverage
  - Delay fault (stuck-at 0/1, stuck open)
  - Bridging between paths under test (PUTs)
  - Latent defects (resistive opens)
- Localize faulty resources
  - Fault diagnosis for process improvements
  - Application-specific FPGA model

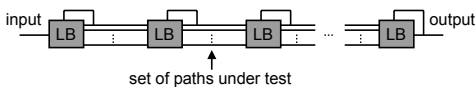
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## Interconnect Delay Fault Test Overview

- Configure FPGA into chains of logic blocks
  - Two cfgs. needed for  $\uparrow$  and  $\downarrow$  faults
- PUTs have same propagation delays
  - Create race between signals
- Delay sensitivity adjustable via feedback path
  - Lower detection limit 2-3 k $\Omega$  resistive open



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## Interconnect Delay Fault Test Implementation

- Two latches, initially transparent
- Measure phase difference between signals
- *First* signal propagates through one latch
  - Fed back to the clock input: closes latches
- *Last* signal input to other latch
  - Propagates if phase difference small
  - Blocked if phase difference large
- Fault detected when *Last* Signal blocked
- Test result stored in latch

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## Resistive Open Defects Detection Sensitivity

- Using RC model, fastest speed grade device
- $R_{\text{defect}} = \text{max. tolerable PUT defect resistance}$

Device	$R_{\text{defect}}^1$
Spartan-II	3.6
Virtex	4.7
Virtex-II	3.5
Virtex-E	2.0
Virtex-IIPro	4.0
units	k $\Omega$

<sup>1</sup>C<sub>segment</sub> approximated as .5 pF

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## Bridging Faults Detection

- Signals on adjacent PUTs are always opposite polarity
  - Wired-AND/OR will make signals equal
- Premature transition on one PUT
  - Large *First-to-Last* signal phase difference
  - Behaves like delay fault

Chmelar, E. "FPGA Interconnect Delay Fault Testing", <http://crc.stanford.edu/~munda/pubs.html>, submitted to ITC'03, 2003.

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