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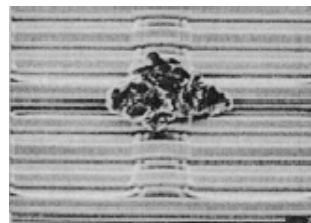
Subframe Multiplexing: Test Configuration Time Reduction

Erik Chmelař
Stanford University
February 2004

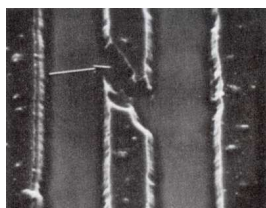
FPGA Manufacturing

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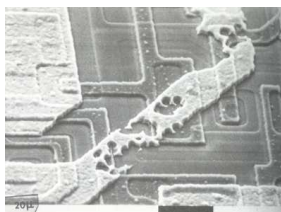
- Integrated circuit manufacturing
 - Imperfect
 - ★ Device defects
- Manufacturing test
 - Detect defects



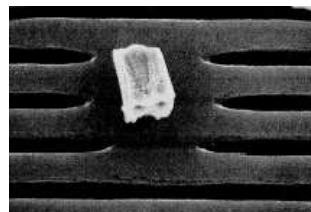
[R&D Mag., 1994]



[Hi-Rel Labs, Inc.]



[Hnatek, 1987]



[Maly, 1987]

Manufacturing Test

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- Iterate
 - Configure device
 - ★ Test configuration
 - Apply test vectors
 - Observe output response
- Billions of possible configurations
 - Configurable interconnection network
- Adequate defect coverage
 - ☹ Many test configurations



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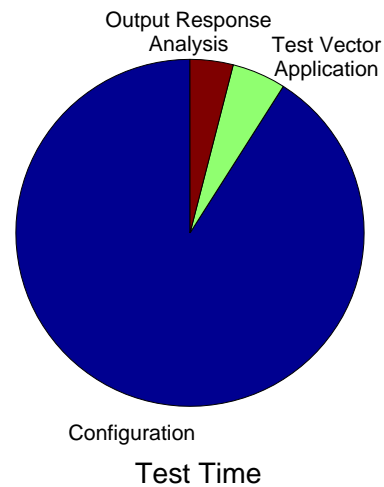
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Test Time

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- Time = \$\$\$
- Configuration
 - Slow
 - ★ 4–8 ms per configuration
- Test stimulus and response
 - Fast
 - ★ μ seconds per configuration



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Test Time Reduction

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- Reduce number of test configurations
 - Logic resources
 - ★ [Renovell et al., 1999a] [Renovell et al., 1999b]
[Renovell et al., 1997]
 - Routing resources
 - ★ [Tahoori and Mitra, 2003] [Sun et al., 2002a]
[Sun et al., 2002b]
- Reduce number of external device configurations
 - [Doumar and Ito, 1999]
- ☺ Reduce configuration time

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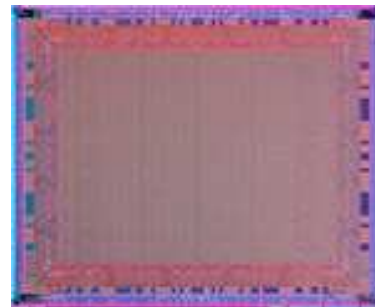
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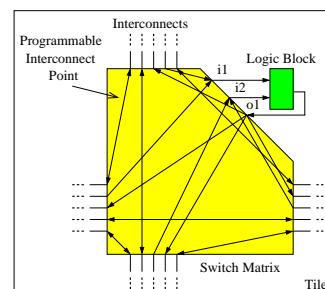
FPGA Structure

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- Very regular structure
 - Array of tiles
 - ★ Replication of identical tiles
- Tile
 - Switch matrix
 - ★ Programmable interconnect points
 - Logic block or input/output block
 - Local routing



Spartan-3 [Xilinx, Inc.]



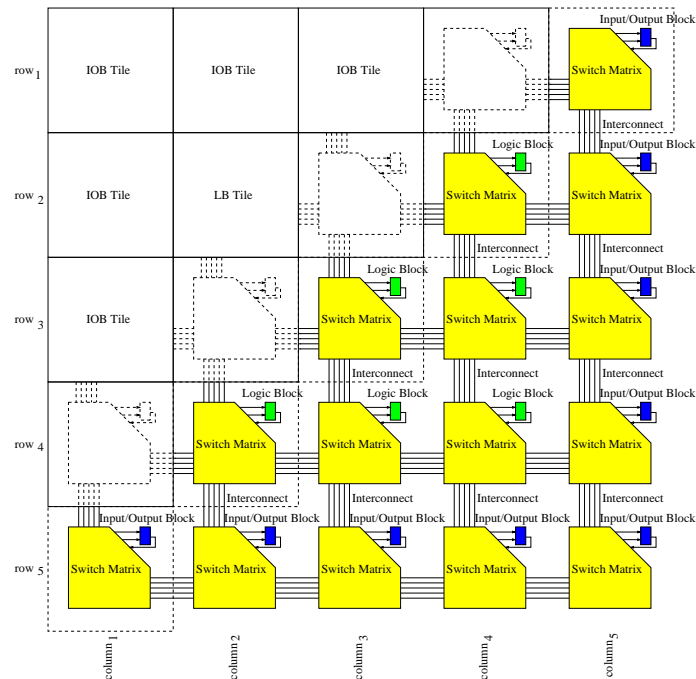
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Tiled Layout

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Test Configurations

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- Very regular
 - Based on tiled FPGA structure
- Stamping
 - Design configuration for one tile
 - Replicate configuration over all identical tiles
- Templating
 - Design configuration using specific resources in each tile

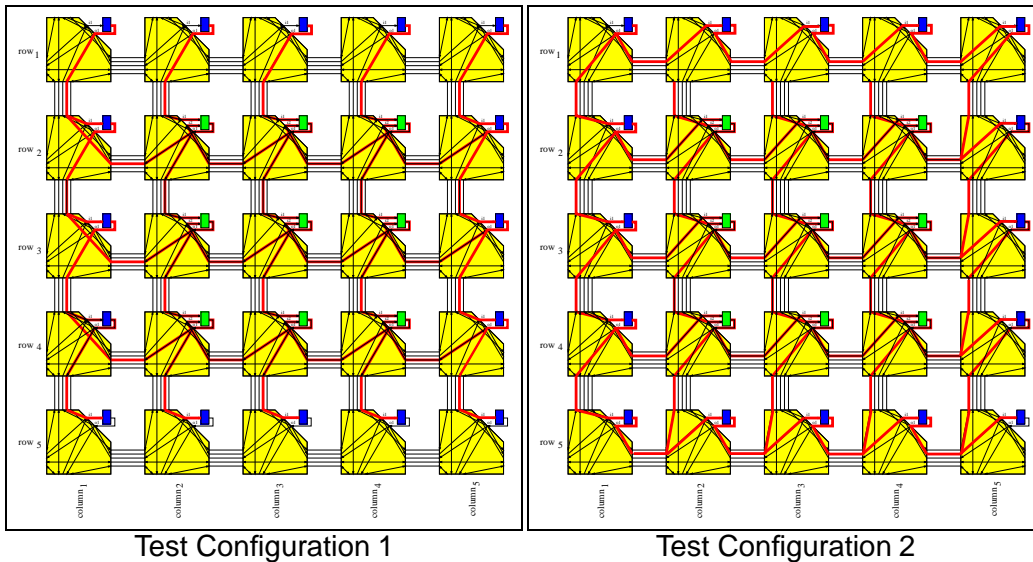
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Tiled Test Configurations

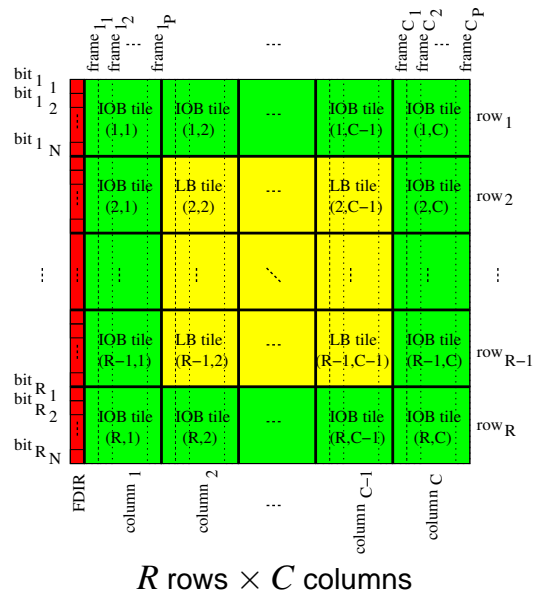
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Configuration Hardware

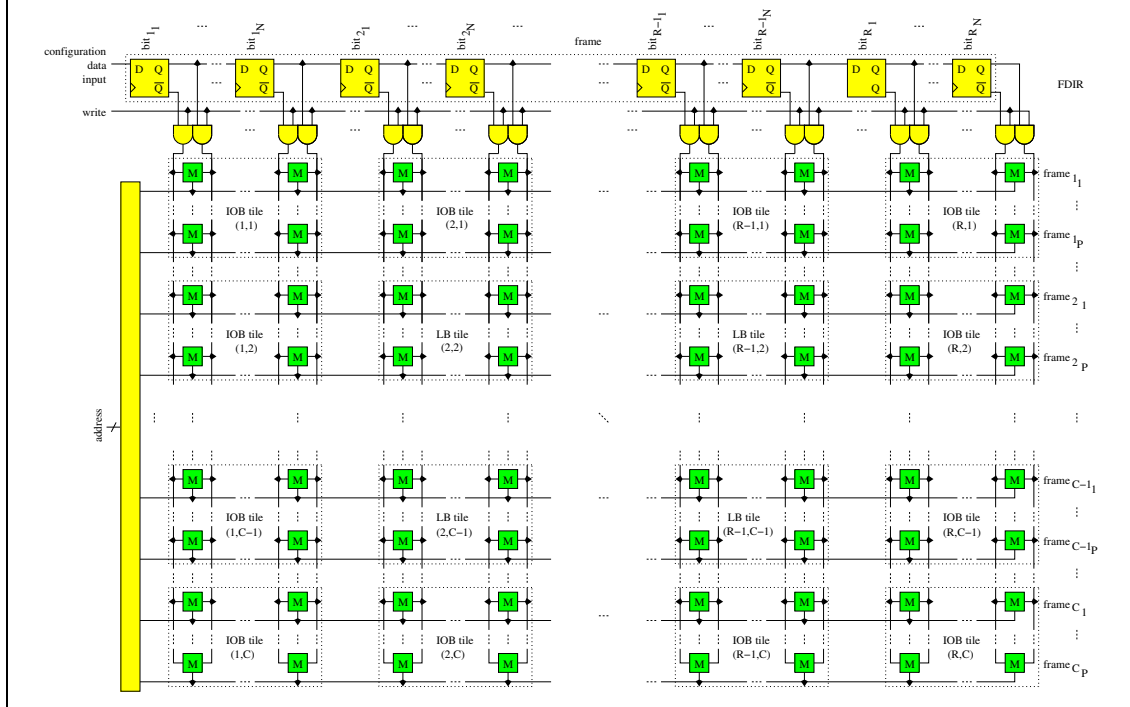
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- Configuration Memory
 - Distributed SRAM cells
 - Organized by *frames*
 - ★ 1-bit wide
 - ★ Spans height of FPGA
 - P frames per column
- Frame Data Input Register
 - Stores data for one frame
 - ★ Serial shift-in
 - ★ Parallel shift-out



Configuration Memory (sideways)

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Standard Device Configuration

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- Shift each frame into FDIR serially
 - aRN units of time
 - ★ a units of time per bit shift-in
 - ★ R rows \times N bits per row
- Shift each frame out to memory location in parallel
 - bCP units of time
 - ★ b units of time per frame shift-out
 - ★ C columns \times P frames per column
- Total configuration time
 - $\Theta(aRN + bCP)$ units of time

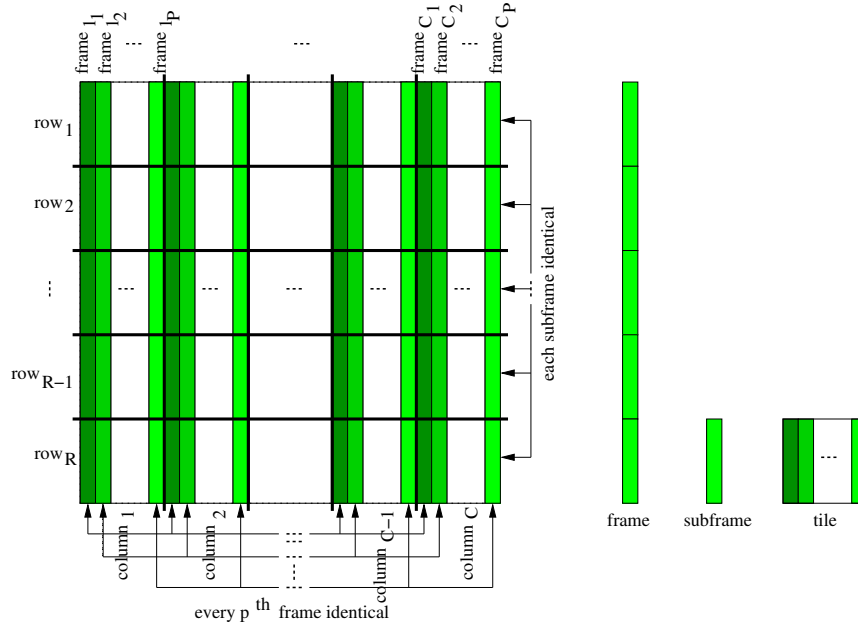
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Test Configuration Data

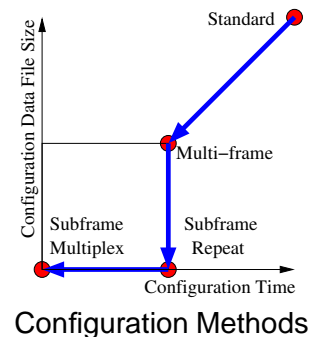
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Improved Device Configuration

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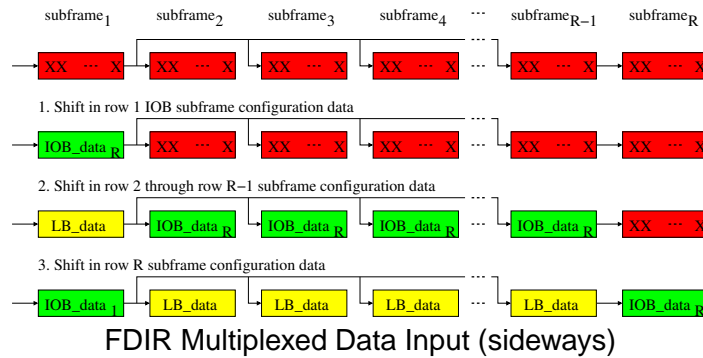
- Multi-frame
 - Configuration time reduction
 - ★ Shift frame out to multiple memory locations
- Subframe Repeating
 - Configuration data file size reduction
 - ★ Store identical subframes once
 - ☹ Must shift *every* subframe into FDIR
- ☺ Subframe Multiplexing
 - Configuration time reduction
 - Shift identical subframes into FDIR in parallel



Subframe Multiplexing

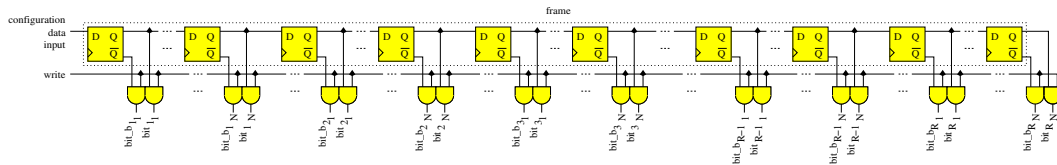
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- Divide frame into R subframes
- Modify frame data input register
 - Add $R - 3$ 2-bit multiplexers
- Shift identical subframes into FDIR in parallel

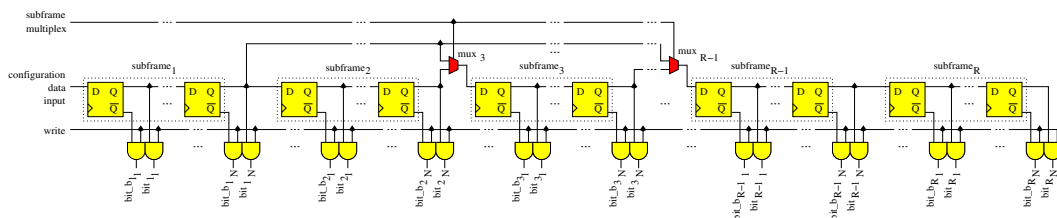


Frame Data Input Register (sideways)

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Original FDIR

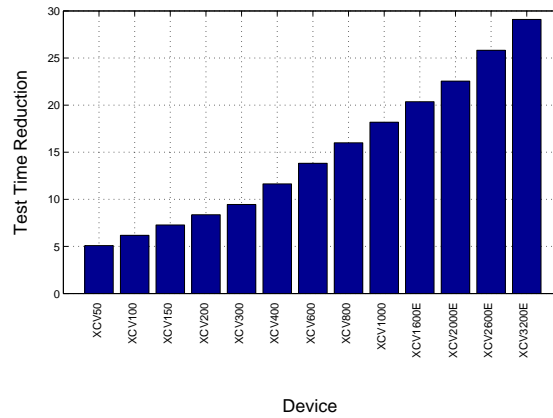


Modified FDIR

Subframe Multiplexing Results

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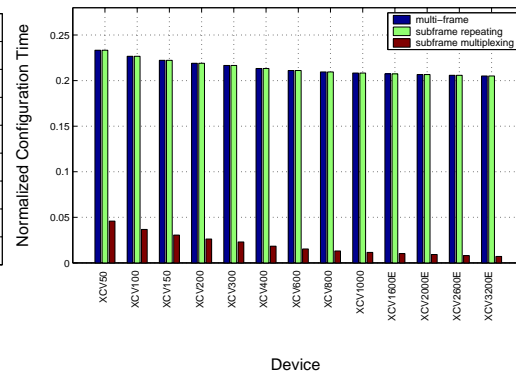
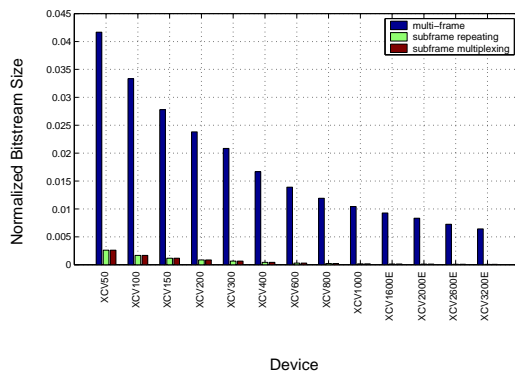
- Reduced configuration time vs. best known method
 - Function of device size
 - ★ 5x reduction for XCV50
 - ★ 30x reduction for XCV3200E



Configuration Methods Comparison

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Method	Configuration Data (bits)	Configuration Time (arbitrary units of time)
standard	$\Theta(RNCP)$	$\Theta(aRN + bCP)$
multi-frame	$\Theta(RNP)$	$\Theta(aRN + bP)$
subframe repeat	$\Theta(NP)$	$\Theta(aRN + bP)$
subframe mux	$\Theta(NP)$	$\Theta(aN + bP)$



References

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- [Doumar and Ito, 1999] Doumar, A. and Ito, H. (1999). Testing the logic cells and interconnect resources for FPGAs. *Proc. Eighth Asian Test Symp.*, pages 369–374.
- [Hnatek, 1987] Hnatek, E. (1987). *Integrated Circuit Quality and Reliability*, volume 41. Marcel Dekker.
- [Maly, 1987] Maly, W. (1987). Realistic fault modeling for vlsi testing. *Proc. 24th Design Automation Conf.*, pages 173–180.
- [R&D Mag., 1994] R&D Mag. (1994). *R&D Magazine*.
- [Renovell et al., 1997] Renovell, M., Portal, J., Figueras, J., and Zorian, Y. (1997). Test pattern and test configuration generation methodology for the logic of RAM-based FPGA. *Sixth Asian Test Symp.*, pages 254–259.
- [Renovell et al., 1999a] Renovell, M., Portal, J., Figueras, J., and Zorian, Y. (1999a). Minimizing the number of test configurations for different FPGA families. *Proc. Eighth Asian Test Symp.*, pages 363–368.
- [Renovell et al., 1999b] Renovell, M., Portal, J., Figueras, J., and Zorian, Y. (1999b). Test configuration minimization for the logic cells of SRAM-based FPGAs: a case study. *Proc. European Test Workshop*, pages 146–151.
- [Sun et al., 2002a] Sun, X., Alimohammad, A., and Trouborst, P. (2002a). Modeling of FPGA local/global interconnect resources and its derivation of minimal test configurations. *Proc. 17th IEEE Int. Symp. Defect and Fault Tolerance*, pages 284–292.
- [Sun et al., 2002b] Sun, X., Xu, J., Alimohammad, A., and Trouborst, P. (2002b). Minimal test configurations for FPGA local interconnects. *Canadian Conf. Computer and Electrical Engineering*, 1:427–432.
- [Tahoori and Mitra, 2003] Tahoori, M. and Mitra, S. (2003). Automatic configuration generation for FPGA interconnect testing. *Proc. 21st VLSI Test Symp*, pages 134–139.