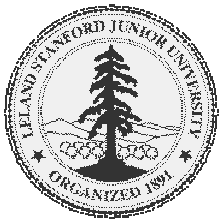

Minimizing the Number of Test Configurations for FPGAs*

Erik Chmelar
LSI Logic
November 10, 2004

***Work done at the Center for Reliable Computing at Stanford University.**

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Outline

- ***FPGA Architecture***
- Background
- Test Configuration Minimization
- Conclusion

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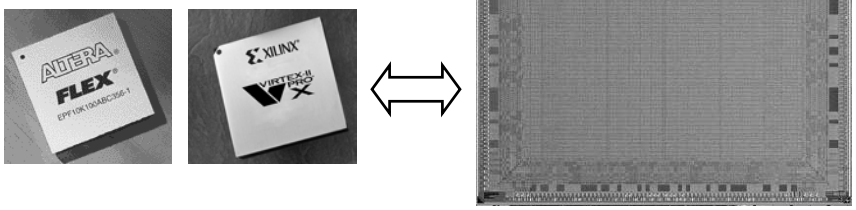
Field-programmable Gate Array

- (Re)configurable integrated circuit
  - Implement arbitrary logic design
- Low non-recurring engineering costs
- Fast time to market



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Building Blocks

- Logic Block (LB)
  - Combinational and sequential logic
- Input/Output Block (IOB)
  - Chip input and output
- Switch Matrix (SM)
  - Conditionally joins interconnects
  - Programmable Interconnect Points (PIPs)

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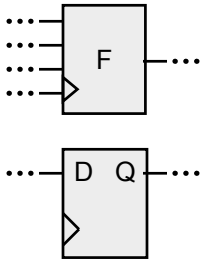
Logic Block

- Look-up Tables (LUTs)
  - Boolean function truth table
- Bistables
  - Flip-flop or latch



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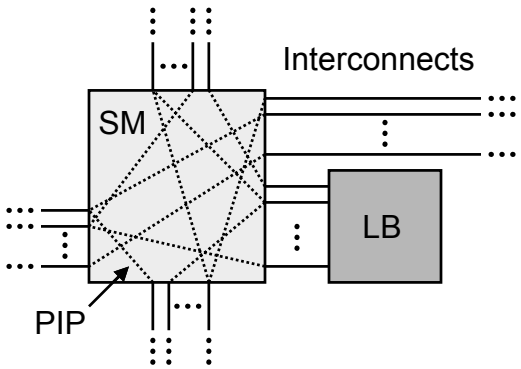
Switch Matrix

- Joins interconnects to
  - Logic Blocks
  - Other interconnects



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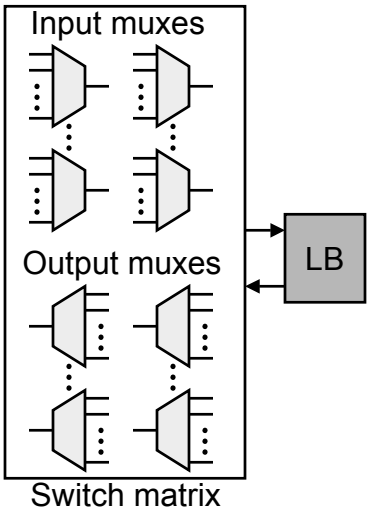
Switch Matrix

- Collection of muxes
  - Input muxes
  - Output muxes
- Various sizes
  - Virtex-II, Spartan-3
    - Largest is 32:1



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Routing Network

- Wire segments
  - Several lengths
  - Grouped into busses
- Programmable Interconnect Points
  - Pass transistor
  - Controlled by SRAM cell
- Buffers
- Vias

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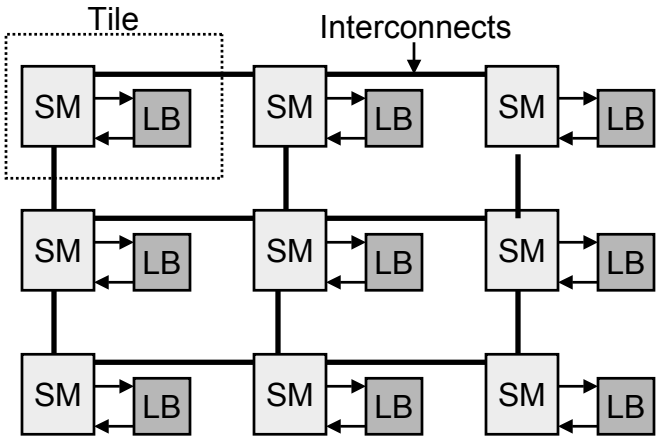
Tiled Layout



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Outline

- FPGA Architecture
- ***Background***
- Test Configuration Minimization
- Conclusion

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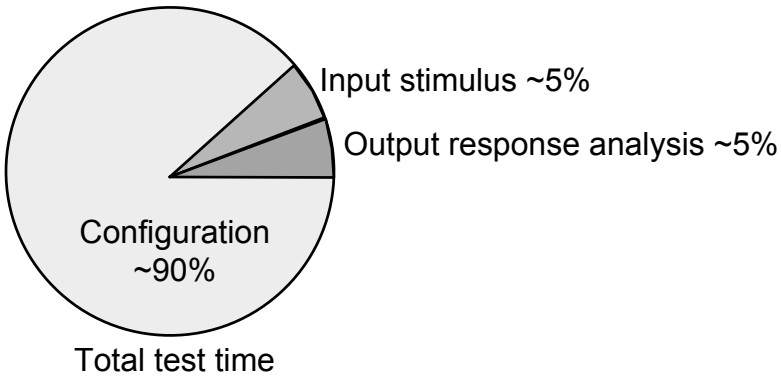
FPGA Test

- Billions of possible configurations
  - How to test them all?
    - Create special test configurations
      - Hundreds used in practice
- Test process

```
do {
    program FPGA with test configuration
    apply test vectors
    compare output to expected value
} until all test configurations used
```


Test Bottleneck

- Configuration time
  - Dominates total test time



Previous Work (1)

- Minimize number of test configurations
  - Represent FPGA as graph
    - Traverse vertices and edges of graph
      - Maximum flow
- Want 100% fault coverage
  - Stuck-at 0/1, PIP stuck-on/off

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Previous Work (2)

- Graph traversal algorithms
  - Virtex architecture
- [Tahoori and Mitra VTS 2003]
  - 8 configurations
    - Not all PIPs considered
    - Input and output muxes not considered
- [Fernandes and Harris ITC 2003]
  - 59 configurations
    - Considers larger subset of routing resources

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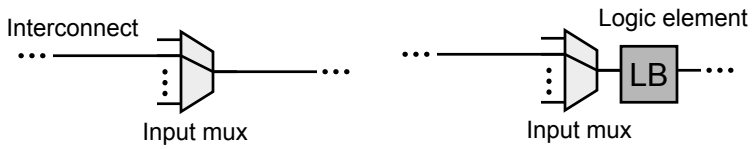
Mux Perspective

- To test all
  - Interconnects
  - Logic element inputs and outputs
    - Signal must traverse input mux
- Necessary and sufficient to test all
  - Input mux inputs and outputs



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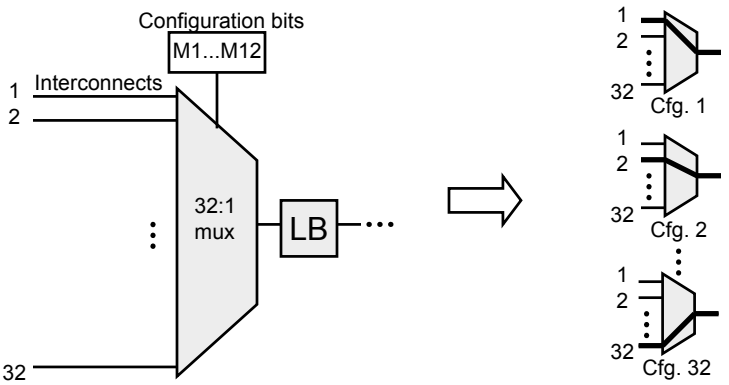
Limitation

- At most one path through mux
  - Minimum *N* configurations for *N*-input mux
    - 32:1 mux → 32 configurations



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Outline

- FPGA Architecture
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- ***Test Configuration Minimization***
- Conclusion

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Solution

- Test
  - Multiple paths through mux per configuration
    - Intentionally short mux inputs
- Reduce number of configurations
  - Less than *N*
- Configuration generation addressed at two levels
  - Mux-level
  - Chip-level

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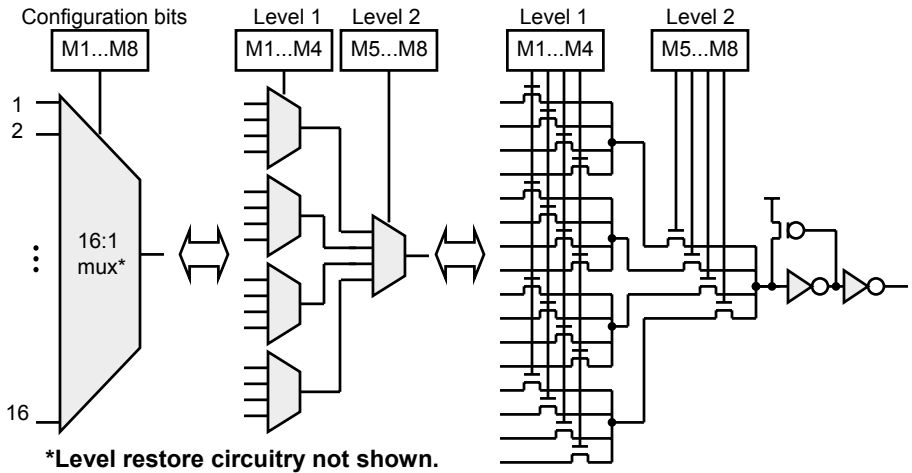
Mux-level Configuration

- Detect all stuck-at 0/1, PIP stuck-on/off faults
- Configure mux
  - Short several mux inputs
- Drive shorted inputs
  - Mux is NMOS pass transistors
    - Strong logic-0
    - Weak logic-1

Mux Implementation

- Two-level NMOS pass transistors



Minimum Configurations

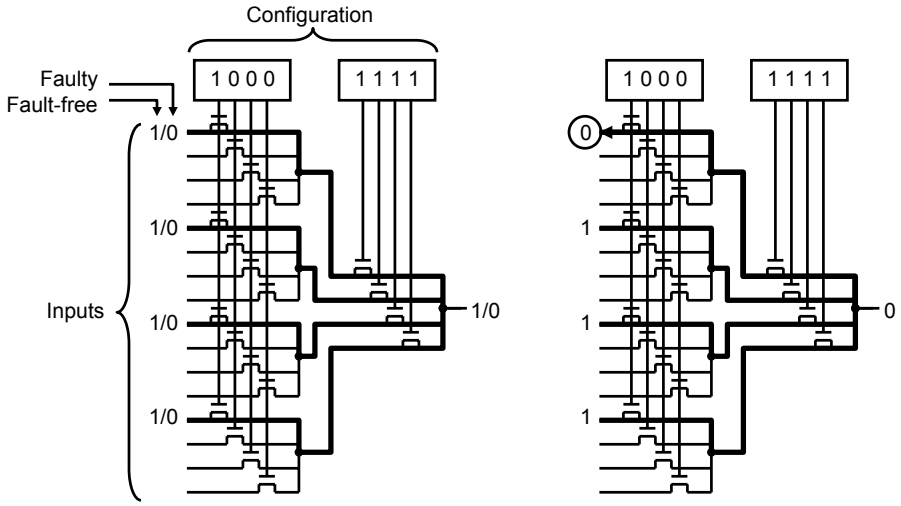
- How to detect stuck-at 0/1 and PIP stuck-on/off?
  - 1 logic-0 input overpowers 4 logic-1 inputs
    - SPICE simulations (90 nm, 1.2 V)
    - Verified on FPGA
  - Condition mux inputs
    - Create pull-down path
      - Output transition or absence of transition

Stuck-at 0 Detection

- Short 4 inputs
  - Drive each to logic-1
    - Stuck-at 0 overpowers other logic-1 inputs
      - Pulls mux output to logic-0

Stuck-at 0 Example

- Inputs 1,5,9,13, and output tested

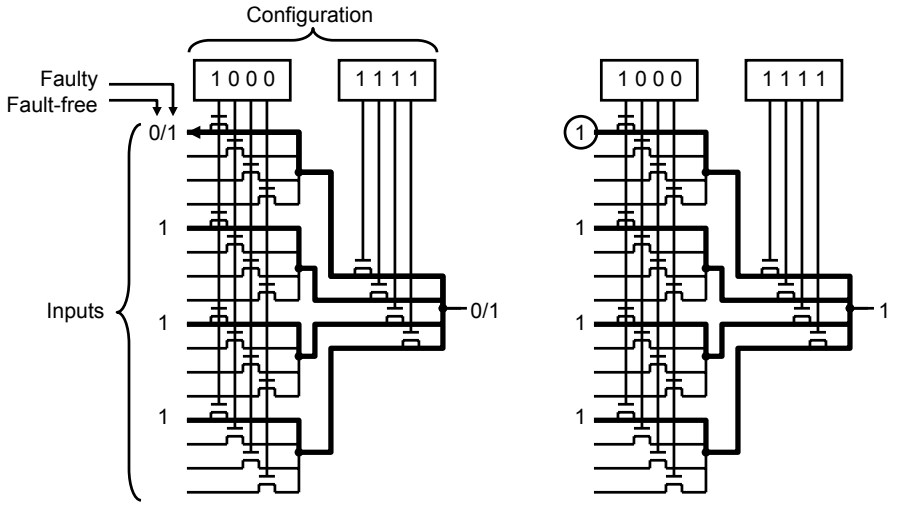


Stuck-at 1 Detection

- Short 4 inputs
  - Drive 3 to logic-1, 1 to logic-0
    - Stuck-at 1 on logic-0 input
      - Mux output remains at logic-1

Stuck-at 1 Example

- Input 1 and output tested



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PIP Stuck-off Detection

- Short 4 inputs
  - Drive 3 to logic-1, 1 to logic-0
    - Stuck-off PIP on logic-0 path
      - Mux output remains at logic-1

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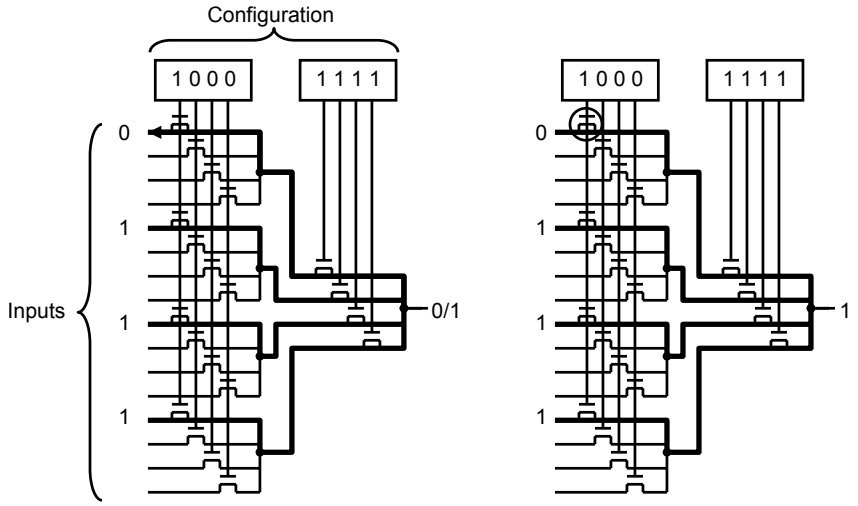
PIP Stuck-off Example

- PIPs 1 and 17 tested



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PIP Stuck-on Detection

- Short 4 inputs
  - Drive all 4 to logic-1, drive others to logic-0
    - Stuck-on PIP on logic-0 path
      - Pulls mux output to logic-0

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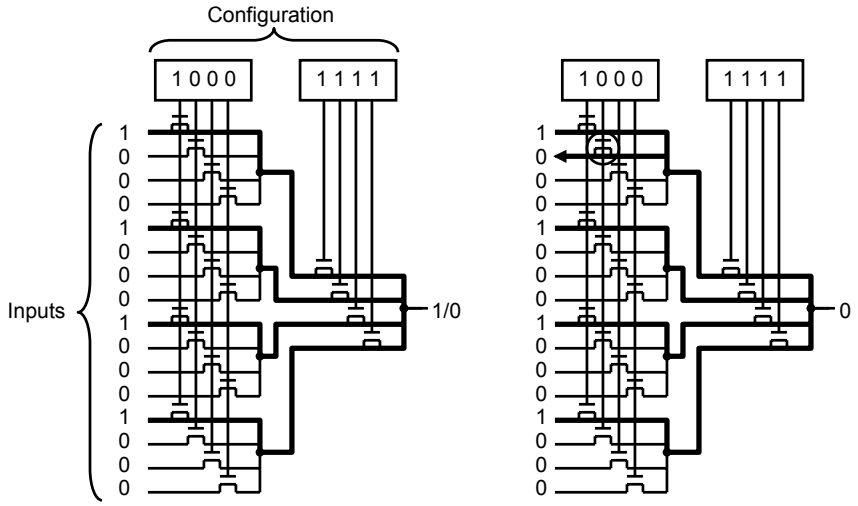
PIP Stuck-on Example

- PIPs 2,3,4, 6,7,8, 10,11,12, 14,15,16 tested

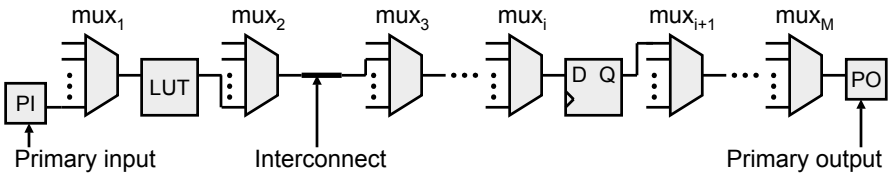


Testing All Inputs and PIPs

- Stuck-at 0/1, PIP stuck-on/off
  - Single mux
    - 6 configurations for 16:1 mux
      - 8 configurations for 32:1 mux
  - All muxes
    - Tested in parallel
      - Still 8 configurations total
        - Join muxes to form Iterative Logic Arrays (ILAs)

Chip-level Configuration

- Control and observe all mux inputs and outputs
- Join muxes to form Iterative Logic Arrays
  - Interconnects
  - Bistables
  - Look-up Tables (LUTs)
- ILA input and output
  - Primary input and output



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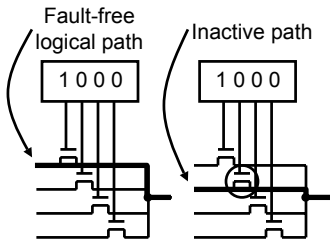
ILA Routing

- Fault-free logical path (FFLP) through mux
  - Path from input to output
    - Through turned-on PIPs
      - No PIP fault present
- Route output of mux_i
  - To FFLP path of mux_{i+1}



- Program bistable to be transparent (D flip-flop)
- Program LUT to propagate fault
  - $F=f(A1,A2,A3,A4)=f_{fault\text{-}free}$ if no fault present
    - $F=\overline{f_{fault\text{-}free}}$ if at least one fault present

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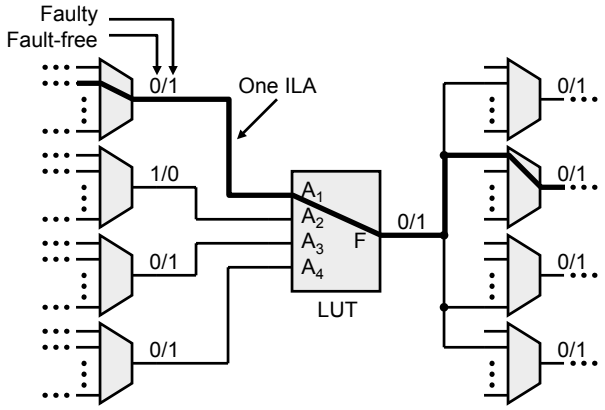
ILA with LUT Example

- *F=(A1'•A2•A3'•A4')'=0*



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Outline

- FPGA Architecture
- Background
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- ***Conclusion***

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Conclusion

- Configuration time dominates FPGA test time
- Minimum number of configurations
  - Limited by size of largest mux
    - One path through mux per configuration
      - 32:1 muxes in Spartan-3, Virtex-II
- Solution
  - Enable multiple paths through mux
    - 8 configurations
      - Detect all stuck-at 0/1, PIP stuck on/off