



FPGA Interconnect Delay Fault Testing

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Purpose

- Test FPGA routing network
 - Contains up to 80% of all transistors
- Test for delay faults
 - Cause timing failures

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Outline

- **FPGA Architecture**
- FPGA Interconnect Delay Fault Testing
- Implementation
- Analysis
- Conclusion

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Building Blocks

- Logic Block (LB)
 - Combinational and sequential logic
 - Look-up Table (LUT)
 - Flip-flop or latch
- Input/Output Block (IOB)
 - Chip input and output
- Switch Matrix (SM)
 - Connects wire segments
 - Programmable Interconnect Points (PIPs)

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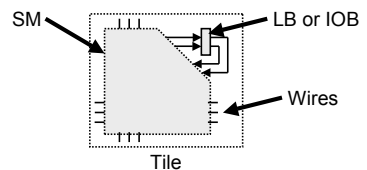
Routing Network

- Wire segments
 - Several lengths
 - Grouped into busses
- Programmable Interconnect Points
 - Pass transistor
 - Controlled by SRAM cell
- Buffers
- Vias

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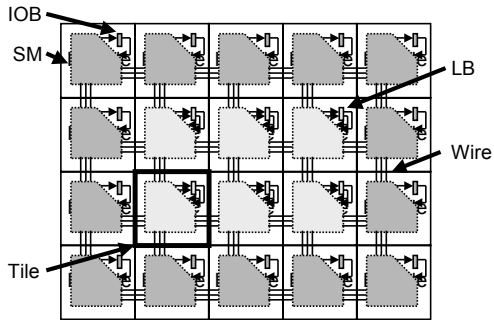
Tile

- Hierarchical grouping
 - Switch Matrix (SM)
 - Logic Block (LB) or Input/Output Block (IOB)
 - Local routing



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Basic Structure



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Test Features

- Detect interconnect delay faults
 - Single or multiple
 - Also detect stuck-at, stuck open, bridging
- Scalable configuration generation
 - Iterative Logic Arrays (ILAs)

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Test Features not Discussed

- Bridging fault detection
- Fault location
 - Diagnosis
 - Application-dependent FPGA model
- FPGA partial reconfiguration
 - Faster total test time

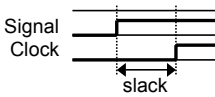
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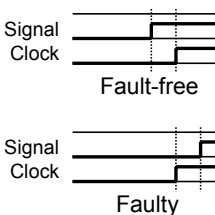
Basic Idea

- Create race on logic block interconnections
 - Paths of equal fault-free propagation delay
- Detect resulting phase difference
 - Phase difference $<$ path slack
 - No delay fault present
 - Phase difference \geq path slack
 - Delay fault detected
- At least one path fault-free

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Fault Definitions

- Path slack:


Signal
Clock
slack
- Delay fault:


Signal
Clock
Fault-free

Signal
Clock
Faulty

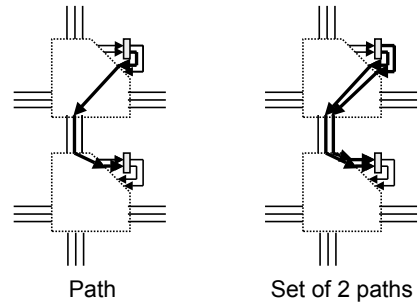
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Test Definitions

- Path
 - Interconnection between LBs
 - PIPs, SMs, wires, buffers, vias
- Set
 - Set of paths
 - Same source and destination LBs
 - Equal fault-free propagation delays
- Iterative Logic Array (ILA)
 - Set and LB concatenation

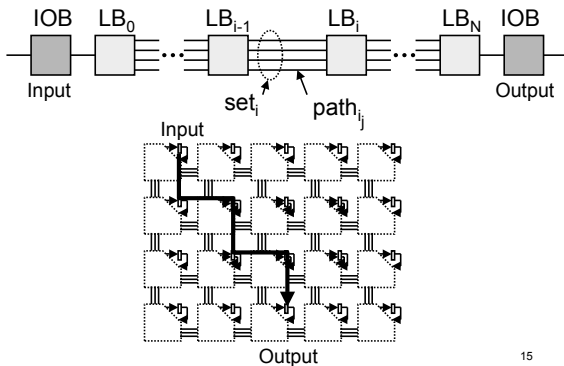
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Path, Set of Paths



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Iterative Logic Array



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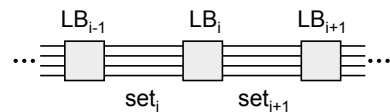
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FPGA Configuration

- Configure FPGA into ILAs
- First LB (LB_0)
 - Initiate race on first set (set_1)
- Intermediate LBs ($LB_1 \dots LB_i \dots LB_{N-1}$)
 - Detect phase difference on set_i
 - Initiate race on set_{i+1}
- Last LB (LB_N)
 - Compact ILA output

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Intermediate Logic Block, LB_i

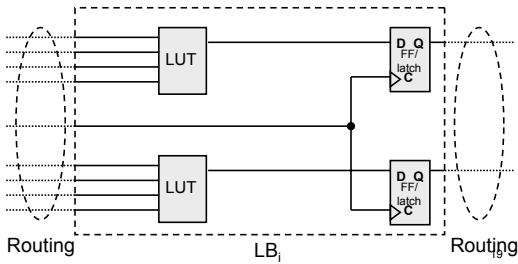


- If set_i fault-free, set_i passes
 - Initiate race on set_{i+1}
- Else if set_i faulty, set_i fails
 - Propagate failure signal on set_{i+1}

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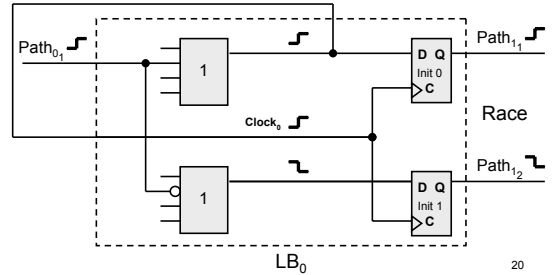
LB Configuration

- Two logic elements (LUTs)
- Two bistables (latch/flip flop)



First Logic Block

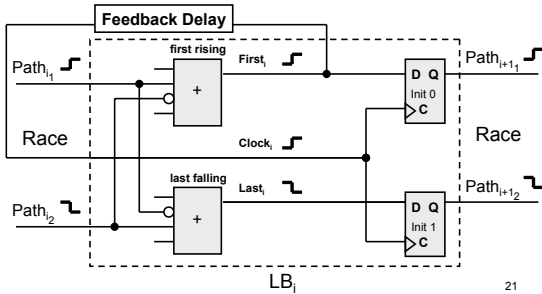
- Single input signal, multiple output signals
- Initiate race on output set



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Intermediate Logic Blocks

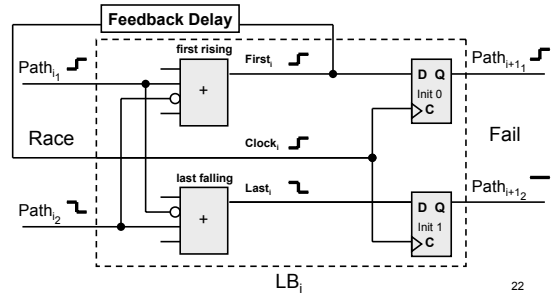
- If input phase difference < path slack
– Initiate race on output set



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Intermediate Logic Blocks

- If input phase difference \geq path slack
– Propagate failure on output set



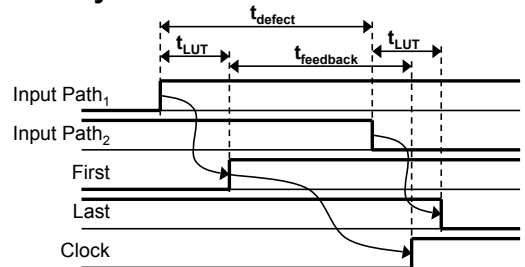
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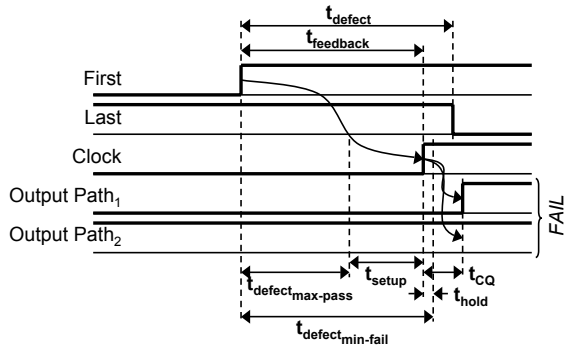
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Faulty Set Phase Detection

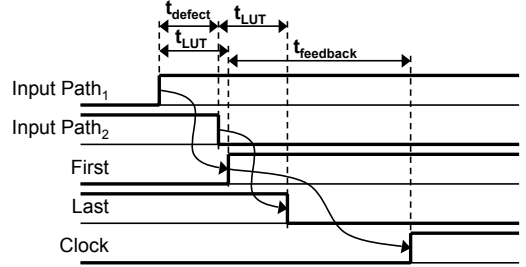


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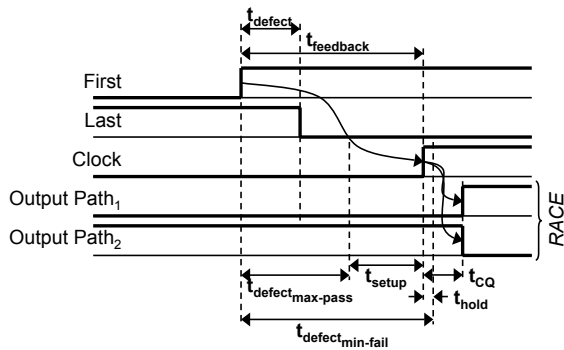
Faulty Set Fail Signal Propagation



Fault-free Set Phase Detection



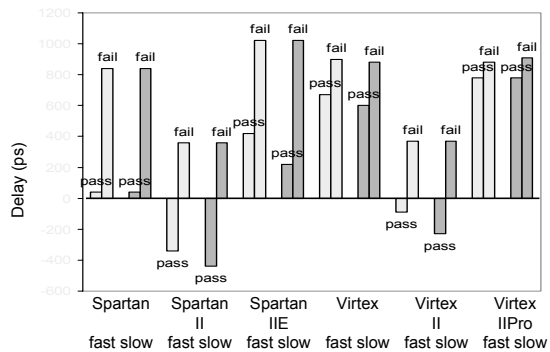
Fault-free Set Race Initiation



Timing Parameters

- $t_{defect_max-pass} = t_{feedback} - t_{setup}$
– Maximum passing phase difference
- $t_{defect_min-fail} = t_{feedback} + t_{hold}$
– Minimum failing phase difference
- $t_{feedback_avg-min}$
– Minimum feedback delay
– Average over all logic blocks

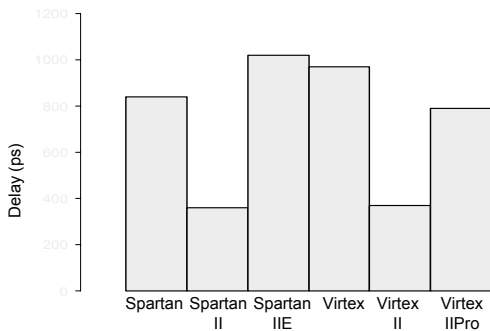
Delay Fault Thresholds



Maximum passing delay < 0 ?

- *Minimum* feedback delay
– Too small
– Device may always fail

Average Minimum Feedback Delay



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Choosing the Feedback Path

- Too short = small feedback delay
 - Test too sensitive
 - False failures
- Too long = large feedback delay
 - Test not sensitive enough
 - Low fault coverage
- Choose detection sensitivity
 - Solve timing equations for t_{feedback}

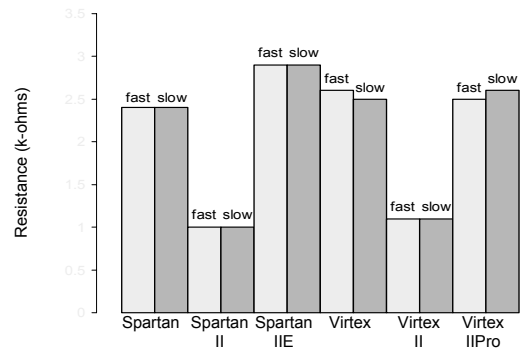
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Resistive Opens

- RC Model
 - Defect resistance
 - Minimum to guarantee detection
 - $$R_{\text{defect, min-fail}} = \frac{t_{\text{defect, min-fail}}}{C_{\text{segment}} \ln(2)}$$

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Minimum Detectable Resistance*



*Capacitance estimated at 0.5 pF

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Conclusion

- Interconnect delay fault test
 - Detect delay faults
 - Timing failures
 - Scalable configuration generation
 - Iterative Logic Arrays
 - Resistive opens
 - 2-3 kΩ maximum sensitivity

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