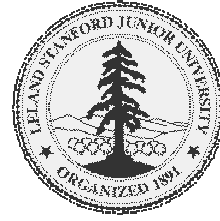


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Exploiting FPGA's Configurability for Testing and Tolerance

Erik Chmelar
Center for Reliable Computing
Stanford University
July 22, 2002

Outline

- ***Introduction***
- FPGA Architecture
- Testing
- Defect Tolerance
- Fault Tolerance
- Conclusion

Introduction

Why FPGAs?

FPGA

- Field (re)programmable
- Highly flexible
- No *NRE* costs
- Short development time

Standard Cell ASIC

- Application specific
- Very inflexible
- High *NRE* costs
- Long development time

[Schrek 99]

Outline

- Introduction
- ***FPGA Architecture***
- Testing
- Defect Tolerance
- Fault Tolerance
- Conclusion

FPGA Architecture

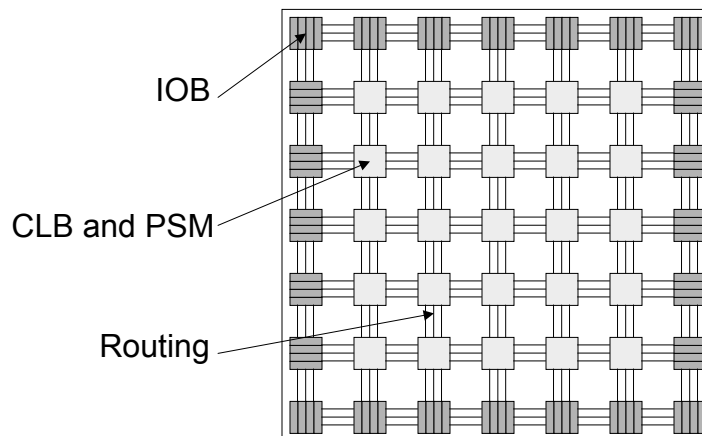
- Basic Building Blocks
 - Configurable Logic Blocks (CLBs)
 - Input/Output Blocks (IOBs)
 - Programmable Switch Matrices (PSMs)
- Routing Resources: > 50% of die area
 - Wires
 - Programmable Interconnect Points (PIPs)

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Basic Building Blocks

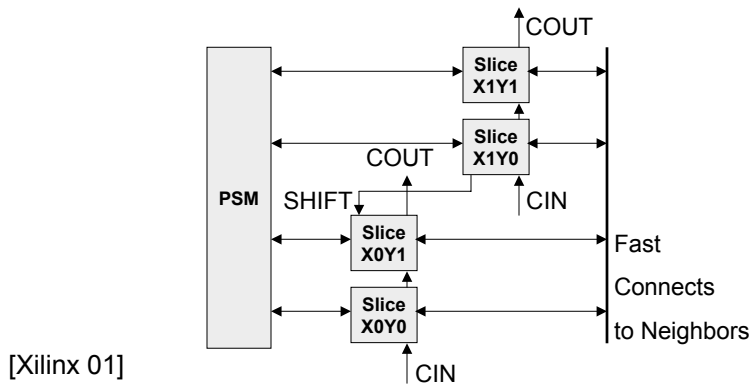


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Configurable Logic Block (1) Xilinx Virtex-II CLB



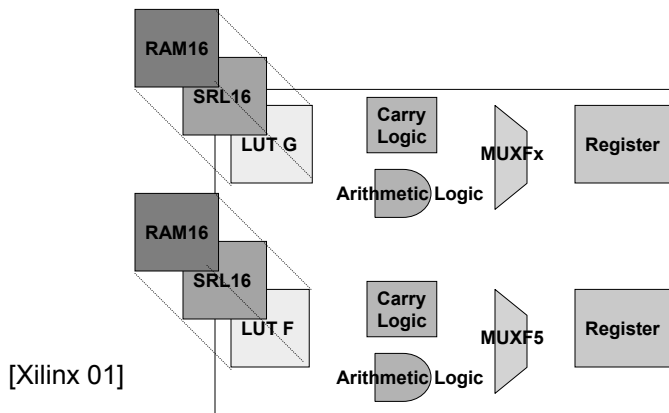
[Xilinx 01]

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Configurable Logic Block (2) Xilinx Virtex-II Slice



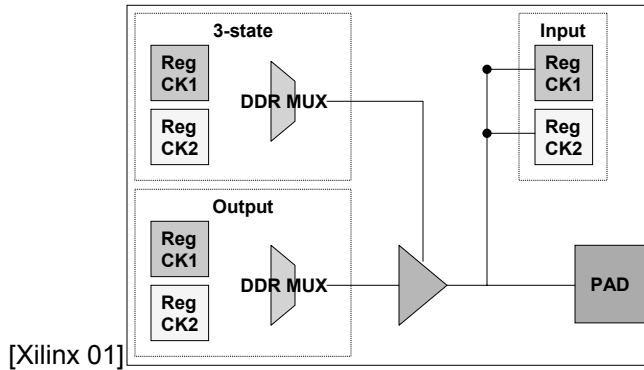
[Xilinx 01]

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Input/Output Block Xilinx Virtex-II IOB

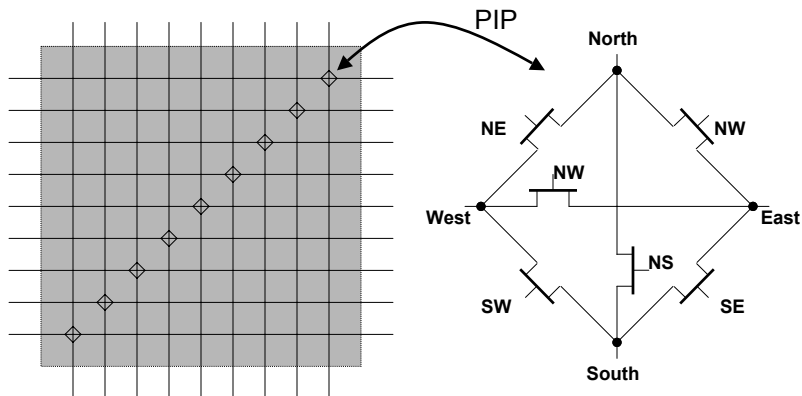


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Programmable Switch Matrix



Six possible connections, NS, NE, NW, SW, SE, WE

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Wires

Xilinx Virtex-II Wires

Horizontal Long Lines Vertical Long Lines	Span entire height/width of device	
Horizontal Hex Lines Vertical Hex Lines	Connects third or sixth CLB in all four directions	
Horizontal Double Lines Vertical Double Lines	Connects first or second CLB in all four directions	
Direct Connects	Connect neighboring vertical, horizontal, and diagonal CLBs	
Fast Connects	Internal to a CLB	

[Xilinx 01]

PSM
 CLB
 Slice

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Programmable Interconnect Point

- Cross-point PIP – multiple pass transistors
 - Connects wires in disjoint routing planes
- Break-point PIP – single pass transistor
 - Connects wires in same routing plane
- Multiplexer PIP – group of cross-point PIPs
 - Connects one of many possible wires

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Outline

- Introduction
- FPGA Architecture
- **Testing**
- Defect Tolerance
- Fault Tolerance
- Conclusion

Testing (1)

- General Test Methodology
- Testing Logic Blocks
- Testing Routing Resources

Testing (2)

- Testing Logic Blocks
 - Standard Testing Practices
 - Iterative Logic Arrays
 - Built-in Self Test
- Testing Routing Resources
 - Bus-based Testing
 - Delay Fault Testing

General Test Methodology

Good Qualities

- Scalable, independent of array size
- Re-usable, thus automatable
- Small amounts of tester memory
- Few programming phases
- Simple test pattern generation
- High fault coverage for logic and routing

[Toutouchi et al. 02] [Huang et al. 98] [Huang et al. 96]

Standard Testing Practices (1)

Test procedure	Test overhead
Configure FPGA with some design	Time consuming, Configuration simulation
Apply test vectors	ATPG, ATE, Patterns not applied at-speed
Analyze response	Fault simulation

Iterate

[Stroud 96]

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Standard Testing Practices (2)

Assessment

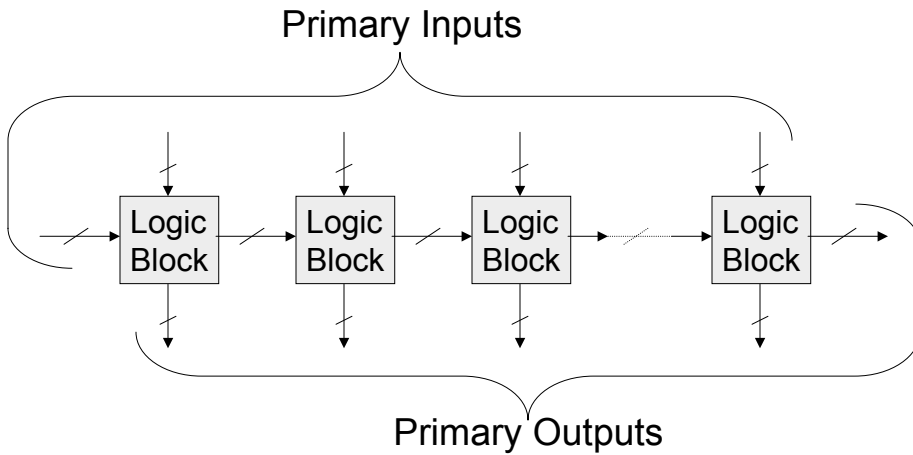
- | | |
|--|----|
| • Scalable, independent of array size | No |
| • Re-usable, thus automatable | No |
| • Small amounts of tester memory | No |
| • Few programming phases | No |
| • Simple test pattern generation | No |
| • High fault coverage, logic and routing | No |

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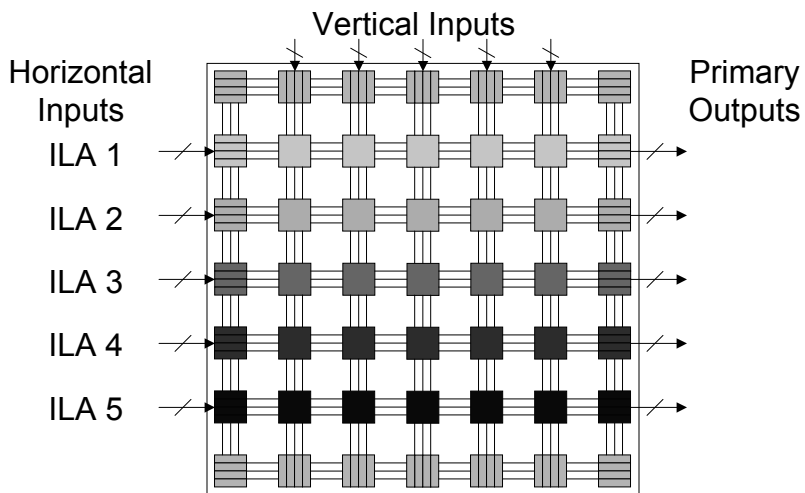
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Iterative Logic Arrays (1)



Iterative Logic Arrays (2)



Iterative Logic Arrays (3)

Assessment

- | | |
|--|-----------|
| • Scalable, independent of array size | Yes |
| • Re-usable, thus automatable | Yes |
| • Small amounts of tester memory | Yes, BIST |
| • Few programming phases | No |
| • Simple test pattern generation | Neutral |
| • High fault coverage, logic and routing | Neutral |

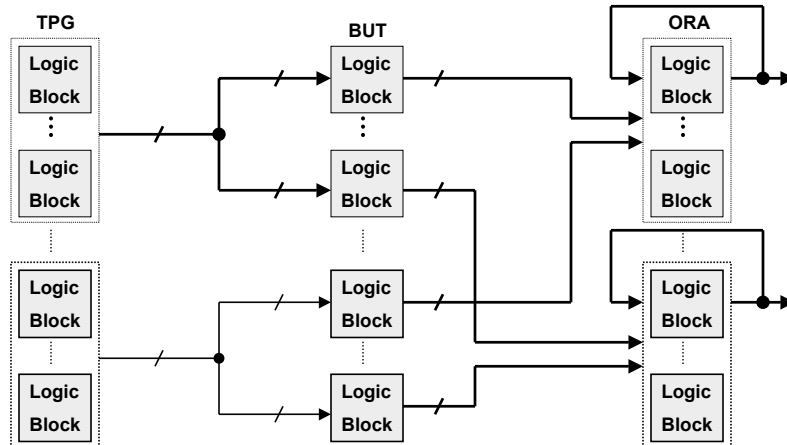
Built-in Self Test (1)

Procedure

- Configuration
 - Block under test (BUT)
 - Test pattern generator (TPG)
 - Output response analyzer (ORA)
- Test pattern generation – TPG
- Test pattern application – TPG, BUT
- Response analysis – BUT, ORA

[Stroud 96]

Built-in Self Test (2)



Built-in Self Test (3)

Assessment

- | | |
|--|------------|
| • Scalable, independent of array size | Yes |
| • Re-usable, thus automatable | Yes |
| • Small amounts of tester memory | Yes |
| • Few programming phases | Yes |
| • Simple test pattern generation | Yes |
| • High fault coverage, logic and routing | Yes, logic |

Bus-based Testing (1)

Routing Resources: PSM

- FPGA Configuration
 - Three PSM configurations needed
- Test pattern application
- Response analysis

[Sun 00]

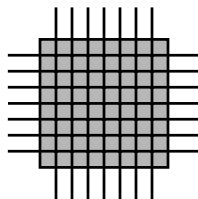
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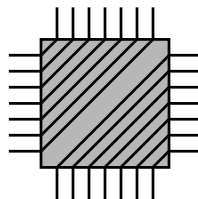
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Bus-based Testing (2)

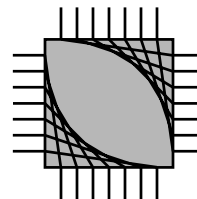
PSM Configurations



Orthogonal
NS, WE



Left-diagonal
NW, SE



Right-diagonal
NE, SW

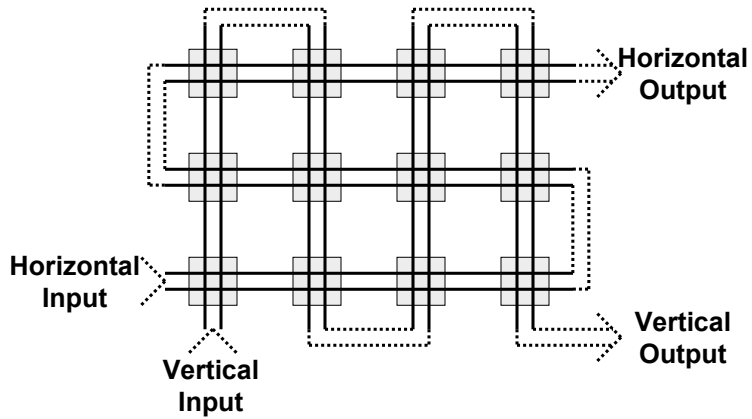
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Bus-based Testing (3)

Example 1: Orthogonal



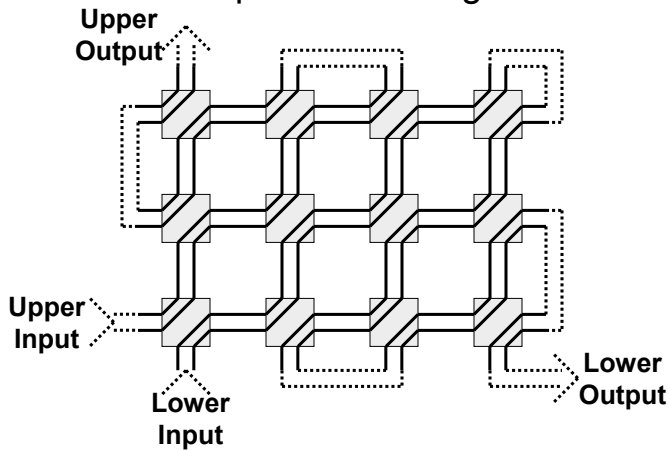
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Bus-based Testing (4)

Example 2: Left-diagonal



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Bus-based Testing (5)

Assessment

- | | |
|--|-----------|
| • Scalable, independent of array size | Yes |
| • Re-usable, thus automatable | Yes |
| • Small amounts of tester memory | Yes, BIST |
| • Few programming phases | Yes |
| • Simple test pattern generation | Yes |
| • High fault coverage, logic and routing | Yes, PSM |

Delay Fault Testing (1)

Routing Resources: Wires

- Targets resistive opens
 - Discontinuity in circuit path
 - 58% returned parts suspect [Needham 98]
- (Circuit) Delay
 - Proportional resistance and capacitance
- Delay ratio $\frac{\text{defective circuit delay}}{\text{equivalent defect-free circuit delay}}$

[Tahoori 02]

Delay Fault Testing (2)

Procedure

- FPGA Configuration
 - Disjoint linear paths
 - Only transparent logic – flip flops, inverters
- Path loading
 - Add fanout branches to paths
- Test pattern application
- Response analysis

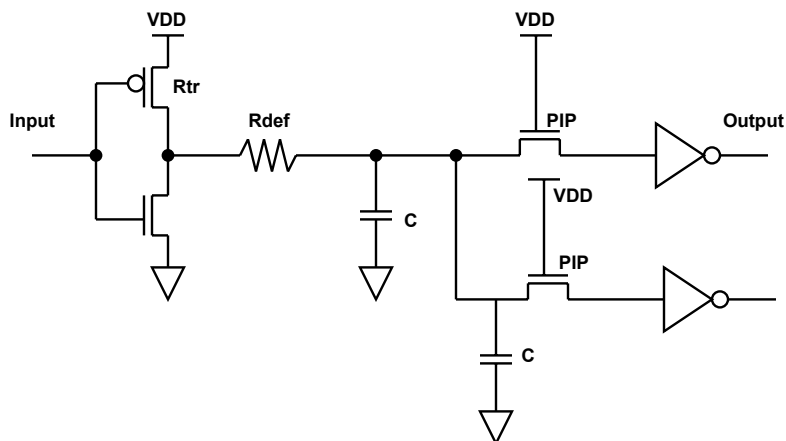
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Delay Fault Testing (3)

$$\text{Delay} \sim [R_{tr}(V_{DD}) + R_{def}] \times C_{total}$$



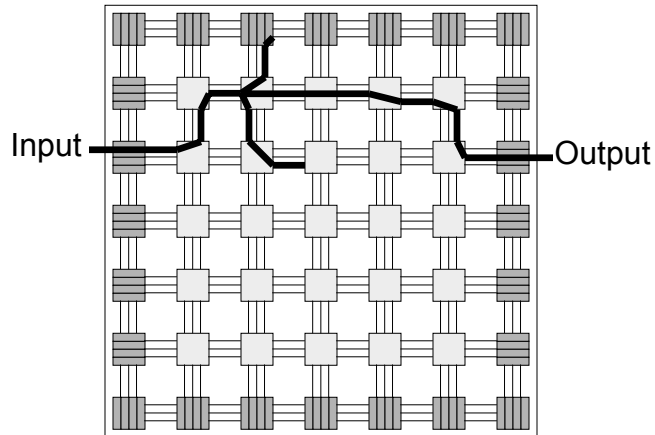
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Delay Fault Testing (4)

Example



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Delay Fault Testing (5)

Assessment

- | | |
|--|------------|
| • Scalable, independent of array size | No |
| • Re-usable, thus automatable | Yes |
| • Small amounts of tester memory | Yes |
| • Few programming phases | No |
| • Simple test pattern generation | Yes |
| • High fault coverage, logic and routing | Yes, wires |

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Outline

- Introduction
- FPGA Architecture
- Testing
- ***Defect Tolerance***
- Fault Tolerance
- Conclusion

Defect Tolerance

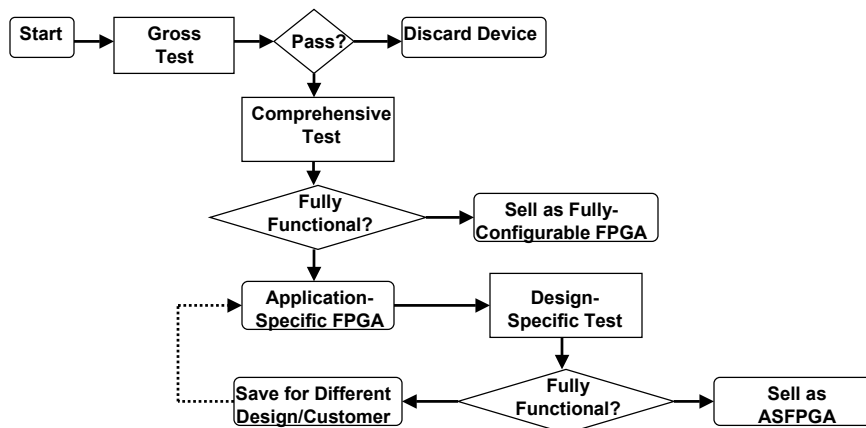
- Application-specific Testing

Application-specific Testing (1)

Overview

- Use known faulty FPGA
 - Avoid faulty resources
- Develop tests based on customer design
- Test FPGA functionality with special test
- Sell FPGA to customer at reduced price
- Effectively increases yield

Application-specific Testing (2)



Outline

- Introduction
- FPGA Architecture
- Testing
- Defect Tolerance
- ***Fault Tolerance***
- Conclusion

Fault Tolerance

- Roving STARS
- Torus Configuration Data Shifting

Roving STARs (1)

Overview

- Find faulty block(s), reconfigure FPGA online
 - Self-testing area (STAR)
 - portion being tested
 - Working area
 - portion implementing normal function
- FPGA remains online

[Stroud 01]

Roving STARs (2)

Requirements

- Runtime reconfigurable (RTR) FPGA
- Spare resources
- Memory to store faulty/not faulty information
- Memory to store precompiled configurations
- Test and reconfigurability controller (TREC)

Roving STARs (3)

Procedure

- Two STARs
 - V-STAR – FPGA column
 - H-STAR – FPGA row
- STARs rove about the FPGA
 - Move to equally-sized areas
 - Configure area for BIST
 - Test the area

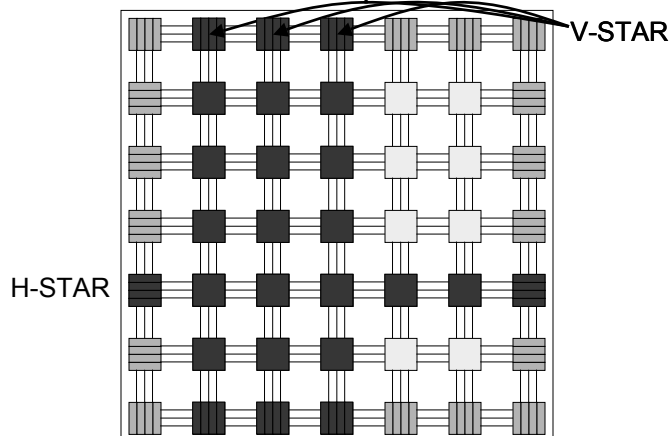
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Roving STARs (4)

Example



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Roving STARs (5)

Issues

- System stalls 3-4 seconds before STAR moves
- Takes long time for STARs to completely rove FPGA
 - 6 minutes to rove 20x20 ORCA 2C15A FPGA

[Emmert 00]

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Torus Configuration Data Shifting (1)

Overview

- Reconfigure FPGA around faulty block(s)
 - Identical unit elements (UEs)
 - Shifts configuration data of UEs
 - north, south, east, or west

[Doumar 01]

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Torus Configuration Data Shifting (2) Requirements

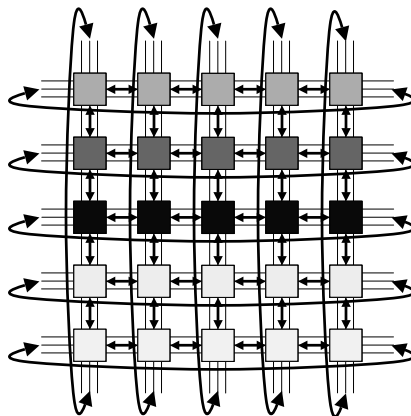
- Modification to standard FPGA structure
 - One 4-input MUX for each memory cell
- Spare UEs
- Memory to store faulty/not faulty information
- Test and reconfigurability controller (TREC)

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Torus Configuration Data Shifting (3) Example: Single Shift North



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Outline

- Introduction
- FPGA Architecture
- Testing
- Defect Tolerance
- Fault Tolerance
- **Conclusion**

Conclusion

- Exploit FPGA reconfigurability
 - For testing
 - Reconfigure sparingly – BIST ILAs
 - For defect tolerance
 - Reconfigure until defect is avoided
 - For fault tolerance
 - Reconfigure until fault is avoided

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