Center for
Reliable
Computing

Possible Testing Methods for Detecting Resistive Opens in FPGA Interconnects

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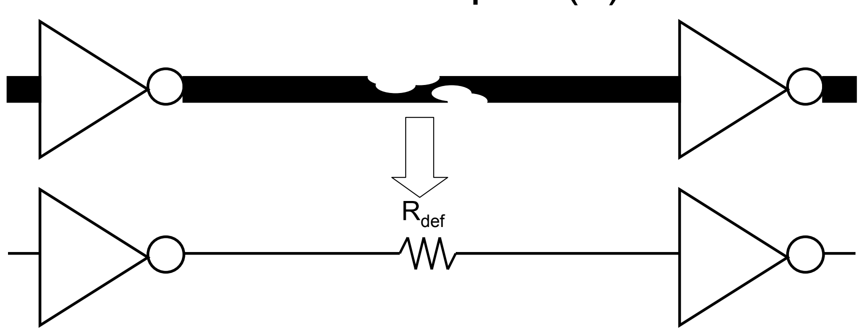
Outline

- ***Background***
- FPGA Architecture
- Induced EMF Testing
- (Two-phase Clock Testing)
- Future Work

Background

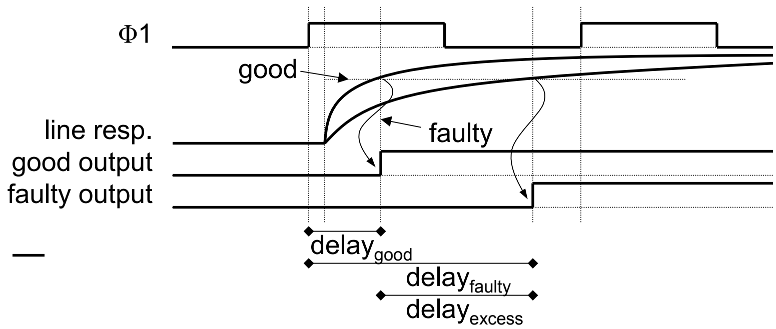
- Effect of resistive open
- Objective

Resistive Open (1)



- Excessive resistance
  - R_{def} varies from ~ 1 Ω to 100 kΩ [Li 02]

Resistive Open (2)



- Circuit delay ~ $[R_{tr}(V_{DD}) + R_{def}] \bullet C$

Objective (1)

Induced EMF Testing

- Induce current [pulse] in an interconnect
  - Detect R_{def} by "measuring" node voltage
  - $I \alpha 1/(R_{line} + R_{def})$, $V \alpha (R_{line} + R_{def})$
    - If V > threshold, R_{def} negligible
    - If V < threshold, R_{def} not negligible
- Current induced by magnetic field gradient dB/dt

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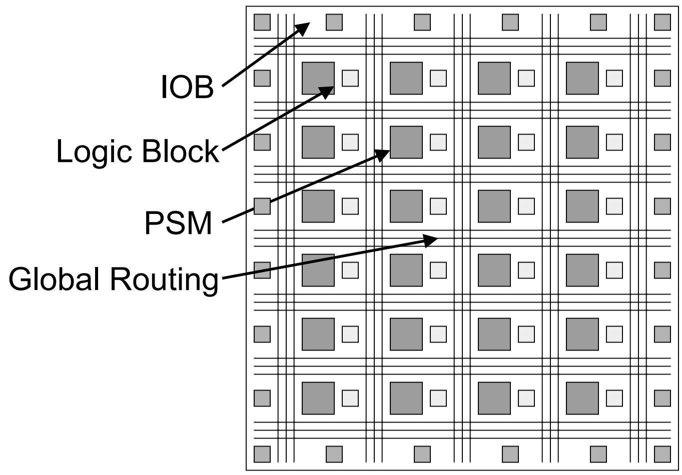
FPGA Architecture

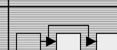
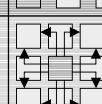
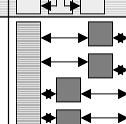
- Basic Building Blocks
  - Configurable Logic Blocks (CLBs)
  - Input/Output Blocks (IOBs)
  - Programmable Switch Matrices (PSMs)
- Routing Resources: > 80% of die area
  - Wires
  - Programmable Interconnect Points (PIPs)

Basic Building Blocks



Wires

Xilinx Virtex-II Wires

Horizontal Long Lines **Vertical Long Lines**	**Span entire height/width of device**	
Horizontal Hex Lines **Vertical Hex Lines**	**Connects third or sixth CLB in all four directions**	
Horizontal Double Lines **Vertical Double Lines**	**Connects first or second CLB in all four directions**	
Direct Connects	**Connect neighboring vertical, horizontal, and diagonal CLBs**	
Fast Connects [Xilinx 01]	**Internal to a CLB**	

PSM **CLB** **Slice**

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Induced EMF Testing (1)

Outline

- Methodology
- Analysis

Induced EMF Testing (2)

Basic Methodology

- Configure FPGA into equally-sized loops
  - Begin at flip-flop (Q output)
  - Traverse [long] lines
  - End at same flip-flop (Clk input)
- Vary magnetic field strength to induce current
  - Causes clock edge at end of loop
- Response saved inside flip-flop*

*Retrieving the response from the flip-flop has not yet been addressed

Induced EMF Testing (3)

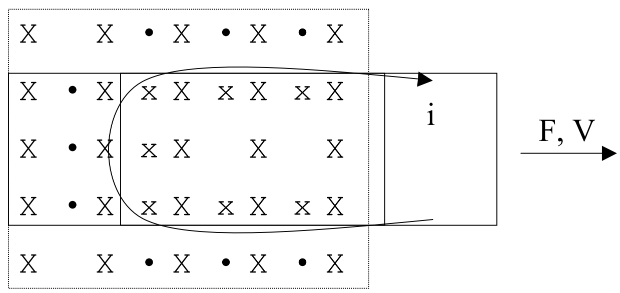
Analysis

- ***Theory***
  - Lenz' Law
  - The loop
  - Magnetic flux
  - Faraday's Law of Induction
  - Ohm's Law
- Implementation

Lenz' Law (1)

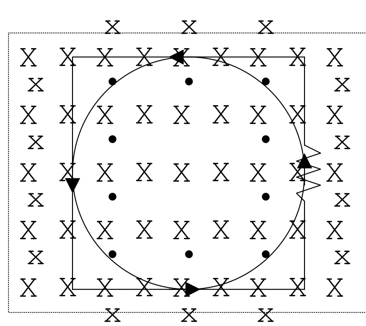
Motional EMF (constant B, varying A)

- *Induced current in a closed loop appears in such a direction that opposes the change that produced it*



Lenz' Law (2)

Non-motional EMF (varying B, constant A)



Loop (1)

Conditions

- Loop must be a *continuous* path
  - Any logic element breaks the loop
    - AOI gates, MUXes, etc...
- Loop actually begins *near* driver
  - Driver output passes through MUX (PSM)
- Loop actually ends *near* driver
  - Input to CLB passes through MUX (PSM)

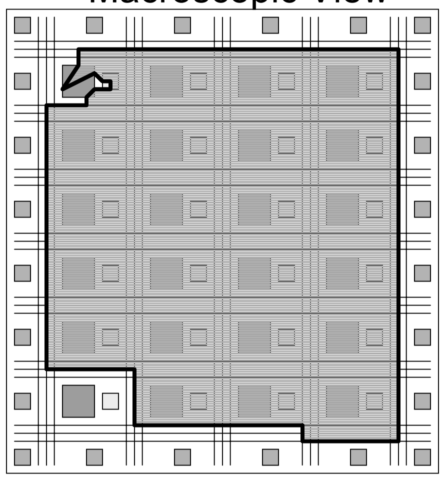
Loop (2)

Carrier Action

- Loop must have driver (current source)
  - Path from V_{DD} or V_{SS}
- When $|dB(t)/dt| > 0$
  - Current flows to maintain constant flux
  - Charges (discharges) capacitance
- When $dB(t)/dt = 0$
  - Current flows via voltage differences
  - Discharges (charges) capacitance

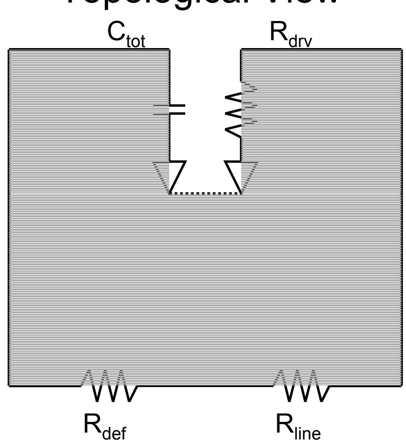
Loop (3)

Macroscopic View

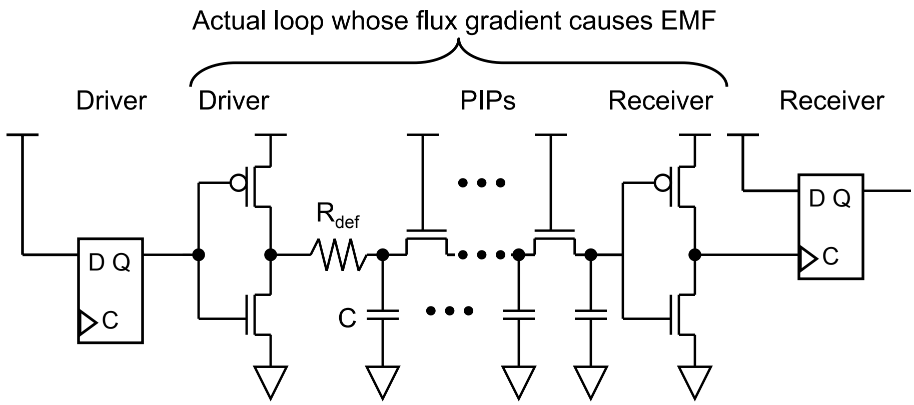


Loop (4)

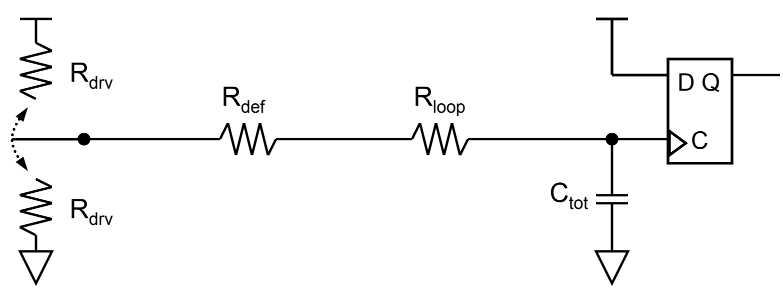
Topological View



Loop (5)
Electrical View



Loop (6)
Functional View



Magnetic Flux

$$\Phi_B(t) = \oint \vec{B}(t) \bullet d\vec{A} \quad \text{magnetic flux}$$

$$= \vec{B}(t) \cdot \vec{A} \cdot \cos\theta \quad \text{dot product}$$

$$= \vec{B}(t) \cdot \vec{A} \cdot \cos 0 \quad \vec{B}(t) \parallel \vec{A}$$

$$= B(t) \cdot A$$

Faraday’s Law of Induction

$$\varepsilon = \frac{-d\Phi_B}{dt} \quad \text{Faraday's Law}$$

$$= \frac{-d(B(t) \cdot A)}{dt} \quad \Phi_B \text{ substitution}$$

$$= -A \cdot \frac{dB(t)}{dt} \quad \text{Area time-invariant}$$

Ohm’s Law

$\varepsilon = i \cdot R$ Ohm's Law

$i = C \dfrac{dV(t)}{dt}$ current into capacitance*

$\varepsilon = R \cdot C \dfrac{dV(t)}{dt}$ i substitution

*Line inductance is considered to be negligible

Derivation (1)

$R \cdot C \dfrac{dV(t)}{dt} = -A \cdot \dfrac{dB(t)}{dt}$ ε substitution

$$\frac{dV(t)}{dt} = -\frac{A}{R \cdot C} \cdot \frac{dB(t)}{dt}$$

$$\frac{dV(t)}{dt} = -\frac{A}{(R_{wires*} + R_{pips} + R_{def}) \cdot C_{tot}} \cdot \frac{dB(t)}{dt}$$

*R_{wires} includes driver, wire, and via resistances

Derivation (2)

$$R_{loop} \approx R_{drv} + \sum_{traversed} (R_{wire} + R_{via} + R_{pip})$$

$$C_{tot} \approx C_{wire} + C_{gate}$$

$$\frac{dV(t)}{dt} = -\frac{A}{(R_{loop} + R_{def}) \cdot C_{tot}} \cdot \frac{dB(t)}{dt}$$

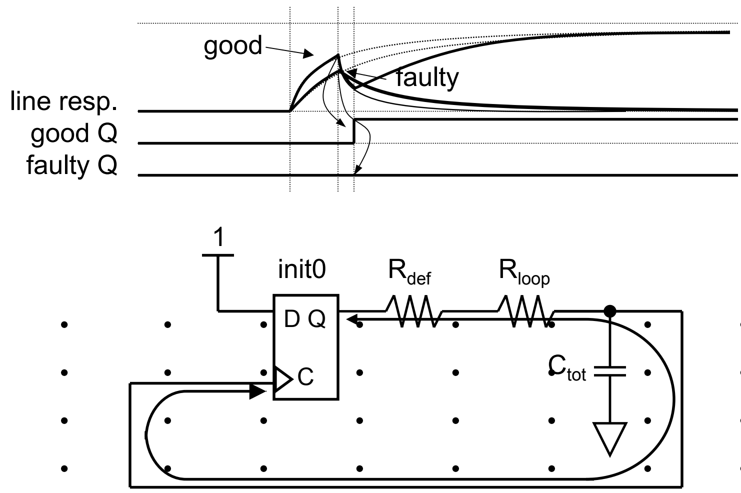
$$\therefore \frac{dV(t)}{dt} = K(R_{def}) \cdot \frac{dB(t)}{dt}$$

Induced EMF Line Testing (3)

Outline

- Theory
- ***Implementation***
  - Example
  - Feasibility analysis
  - FPGA configuration
  - Parasitic effects
  - Advantages

Induced EMF Example



Feasibility Analysis (1)

Approximations

- Area ~ 1 mm^2 to 1 cm^2
  - Die area ranges from ~ 1 to 10 cm^2
- R_{loop} ~ 10 to 100 kΩ
  - Mainly due to PIPs, R_{PIP} ~ .5 to 1 kΩ
- C_{tot} ~ 1 to 10 pF
  - Sum of wire and gate capacitance
- dB/dt ~ 10^4 T/s [Barker 93]

Feasibility Analysis (2)

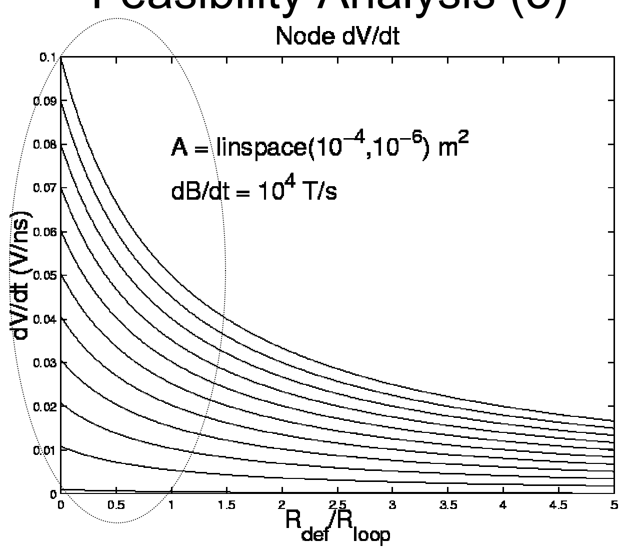
$$\left|\frac{dV(t)}{dt}\right| = \frac{A}{(R_{loop} + R_{def}) \cdot C_{tot}} \cdot \frac{dB(t)}{dt}$$

$$\approx \frac{10^{-4}}{(10^4 + 0) \cdot 10^{-12}} \cdot 10^4 = 10^9 \text{ V/s} = .1\text{V/ns}$$

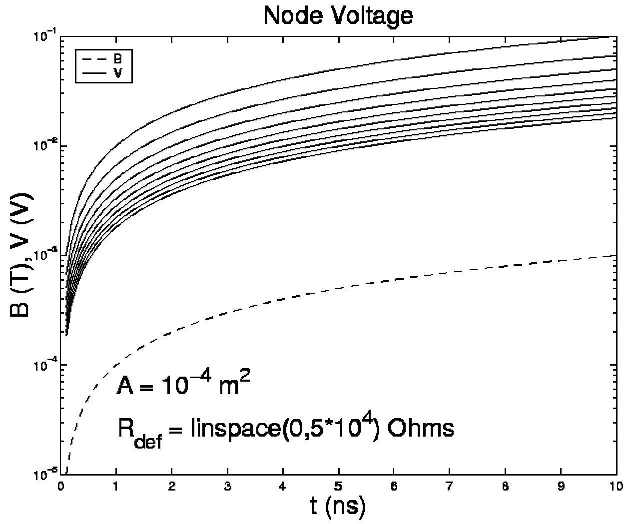
$$\approx \frac{10^{-4}}{(10^4 + 10^3) \cdot 10^{-12}} \cdot 10^4 \approx 9 \cdot 10^7 \text{ V/s} = .09 \text{ V/ns}$$

$$\approx \frac{10^{-4}}{(10^4 + 10^4) \cdot 10^{-12}} \cdot 10^4 \approx 5 \cdot 10^7 \text{ V/s} = .05 \text{ V/ns}$$

Feasibility Analysis (3)

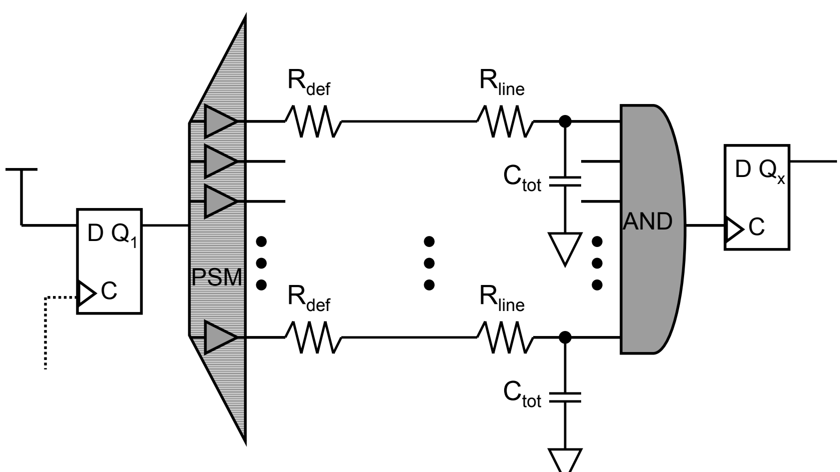


Feasibility Analysis (4)



FPGA Configuration (1)

Realizable Configuration



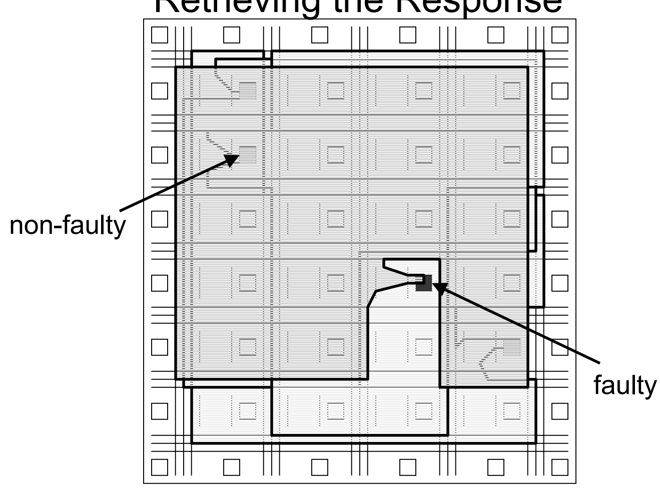
FPGA Configuration (2)

Analysis

- AND gate method
  - Multiple loops tested simultaneously
    - Can be driven by single flip-flop
    - R_{drv} is actually MUX output resistance
  - Each line charges independently
    - $V(t,R_{def}) \alpha 1/(R_{line} + R_{def})$

FPGA Configuration (3)

Retrieving the Response



FPGA Configuration (4)

Retrieving the Response

- Perform serial readback
  - Slow, doesn't scale with array size
- Route to output pins
  - Semi-scalable
- Measure IDDQ
  - Difficult to detect one 'bad' loop among many

Parasitic Effects (1)

Overview

- Is magnetic field damaging to device?
  - Excess current (charge) on tested wires
    - Magnetic field gradient
  - Wires not under test
    - Loops
  - Transistors
    - Lorentz force

Parasitic Effects (2)

Excess Current (Charge) on Tested Wires

- Carefully calculate $K(R_{def})$
  - If $K_{calc}(R_{def}) < K_{actual}(R_{def})$
    - $V_{calc}(t,R_{def}) < V_{actual}(t,R_{def})$
    - Can excessively charge the node
      - Node voltage can charge beyond rails

Parasitic Effects (3)

Wires Not Under Test

- dV(t)/dt is a function of loop area
  - Do not configure untested wires into loops
  - Test with the largest possible loop area
    - Undesired loops should be small
    - $K(A,R_{def}) \alpha A$
      - $A\downarrow \rightarrow K \downarrow \rightarrow dV(t)/dt \downarrow$
    - If unwanted loops exist, dV(t)/dt will be negligible

Parasitic Effects (4)

Transistors

- Electric Fields ~ 1 V/.2 μm = $.5 \times 10^7$ F/m
- Carrier velocity saturates ~ 10^5 m/s
- B_{max} ~ 10^{-4} T (dB/dt = 10^4 T/s = 10^{-5} T/ns: $\Delta V/\Delta t$ = 1 V/10 ns → 10^{-5} T/ns•10 ns = 10^{-4} T)

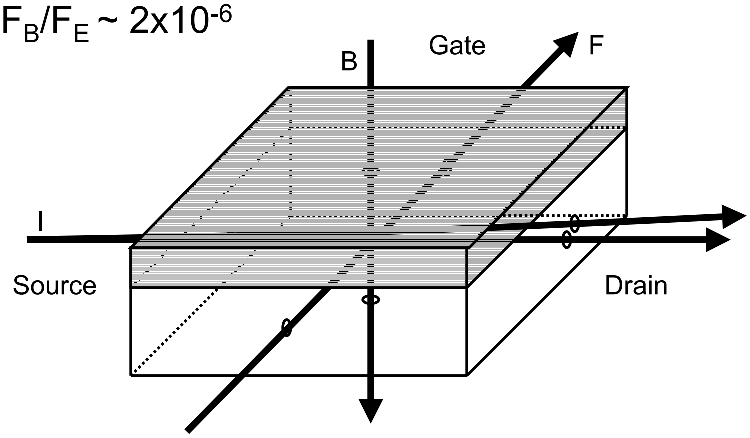
$$F = F_\varepsilon + F_B = q \cdot \varepsilon + q \cdot V \times B \quad \text{Lorentz Force}$$

$$\frac{F_B}{F_\varepsilon} \leq \frac{V \times B}{\varepsilon} \approx \frac{10^5 \times 10^{-4}}{.5 \cdot 10^7} = 2^{-6}$$

Parasitic Effects (5)

Transistors

- F_B/F_E ~ 2×10^{-6}



Advantages

- Arbitrarily small effective clock period
  – No classical concept of clock period
  – No fast external clock needed
  – No clock timing, skew issues
- Induced current sensitive to R_{def}
  – No additional delay elements needed on loop under test (adding paths, etc.)

Outline

- Background
- FPGA Architecture
- Induced EMF Testing
- ***(Two-phase Clock Testing)***
- Future Work

Objective (2)

Two-phase Clock Testing

- Detect R_{def} by reducing clock cycle
  - Two clock phases, Φ1, Φ2
- Toggle a node (interconnect)
  - delay ~ $(R_{line} + R_{def})$•C
    - If delay < Φ2 – Φ1, R_{def} is negligible
    - If delay > Φ2 – Φ1, R_{def} is not negligible

Two-Phase Clock Testing (1)

Outline

- Methodology
- Analysis

Two-Phase Clock Testing (2)

Basic Methodology

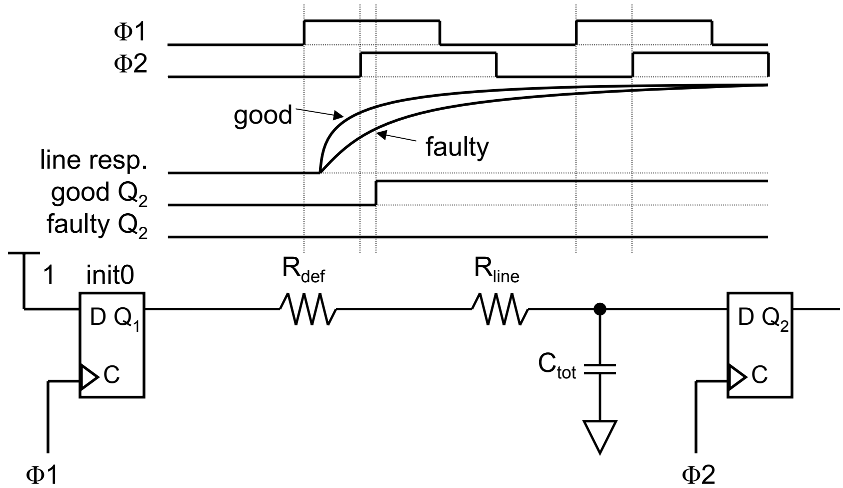
- Configure FPGA into test groups
  - Flip-flop → line → flip-flop
- Clock first flip-flop (Φ1)
- Clock second flip-flop (Φ2)
- Good line: delay < Φ2 – Φ1
- Faulty line: delay > Φ2 – Φ1

Two-phase Clock Testing (3)

Analysis

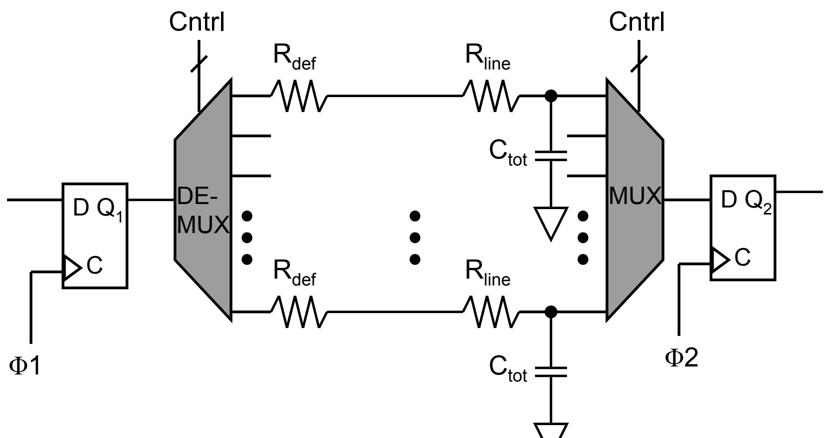
- Application
  - Example
  - FPGA Configuration

Two-Phase Clock Example



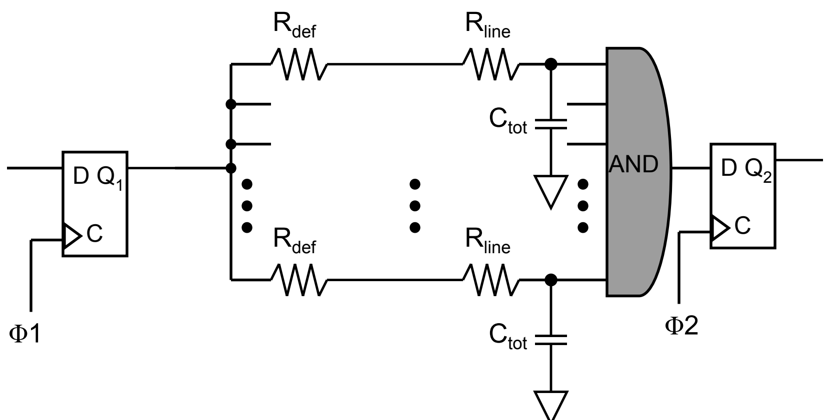
FPGA Configuration (1)

Non-realizable Configuration



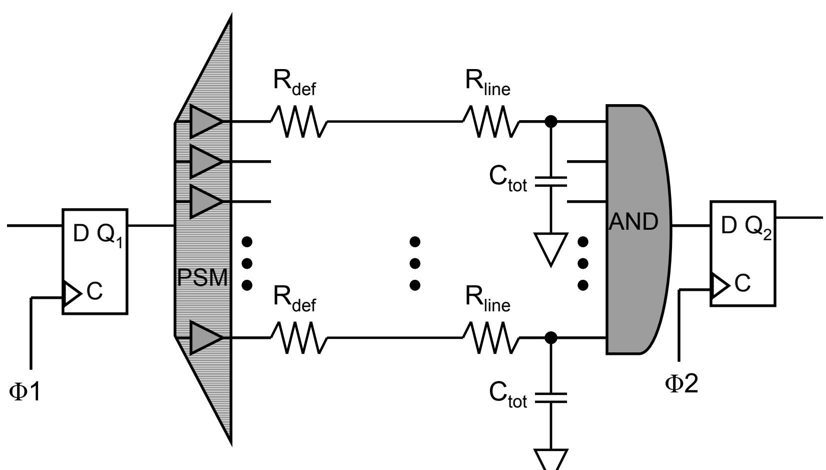
FPGA Configuration (2)

Realizable Configuration: Unbuffered



FPGA Configuration (3)

Realizable Configuration: Buffered



FPGA Configuration (4)

Analysis

- Testing each line individually
  - Many configurations needed
  - DEMUX-MUX method
  - No demultiplexer construct available
- AND gate method
  - Unbuffered: charge time α number of lines
  - Buffered: charge time independent of load

Outline

- Background
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- Induced EMF Testing
- Two-phase Clock Testing
- ***Future Work***

Future Work

- A LOT OF WORK NEEDS TO BE DONE
- Induced EMF Testing
  - Investigate any harmful effects of EMF
  - How to efficiently retrieve the responses
- Two-Phase Clock Testing
  - How to generate clock phases
    - Digital Clock Manager
  - How to ensure precise clock timing

References

[Barker 93] Barker, A.T. “Electricity, Magnetism, and the Body: Some Uses and Abuses.” Engineering Science and Education Journal, Vol. 2 Issue 6, Dec. 1993.

[Li 02] Li, James Chien-Mo. “Test and Diagnosis of Open Defects in Digital CMOS Integrated Circuits.” Ph.D. Thesis, CRC, June 2002.

[Xilinx 01] Xilinx, Inc., San Jose, Ca. “Virtex-II Platform FPGA Handbook,” December 2001.