Center for
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Fast FPGA Interconnect Testing: A New Configuration Architecture

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Outline

- ***Introduction***
- Xilinx Virtex FPGA Structure
- Proposed Method
- Application to Xilinx Virtex
- Previous Work
- Future Work
- Conclusion

Field-programmable Gate Array

- Configurable application-independent device
  - Good for designing
    - Low non-recurring engineering costs
    - Fast development time
  - Bad for testing
    - Long test times
    - Large storage space
    - Difficult test configuration generation

Objective

- Efficient FPGA testing
  - Faster
    - Reduce configuration time
  - Cheaper
    - Reduce ATE time
  - Simpler
    - Simplify configuration generation

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Basic Building Blocks* [Xilinx 02]

- Logic Block (LB)
  - Combinational and sequential logic
- Input/Output Block (IOB)
  - Chip input and output
- Switch Matrix (SM)
  - Connects wires

*Special Block RAM and Multiplier Block are not included

Routing Resources

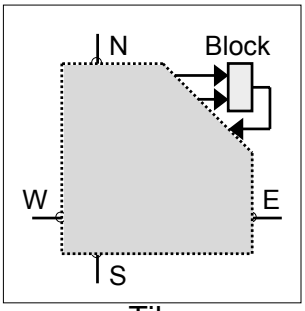
- Wire
  - Various lengths
    - Fast, direct, double, hex, long
- Programmable Interconnect Point (PIP)
  - Pass transistor
    - Controlled by SRAM cell

Configuration Hardware

- SRAM cell
  - Controls PIP
- Configuration data addressing logic
  - Used only during device programming

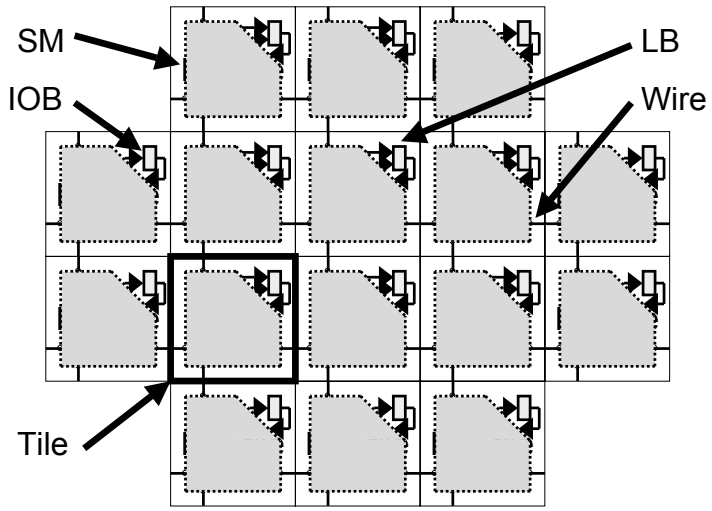
Tile

- FPGA composed of tiles
  - Tile = SM and associated block or blocks
    - LB tile = SM and associated LB
    - IOB tile = SM and associated IOB



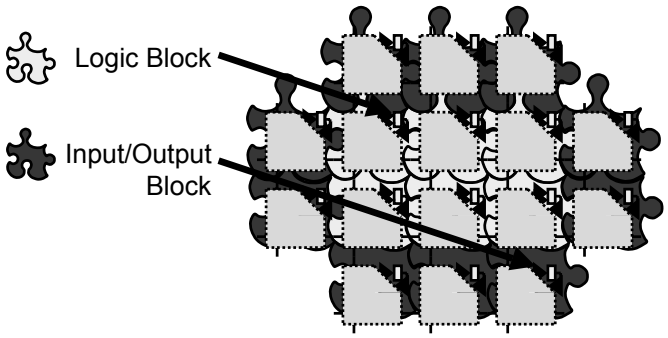
Tile

Tiled Layout



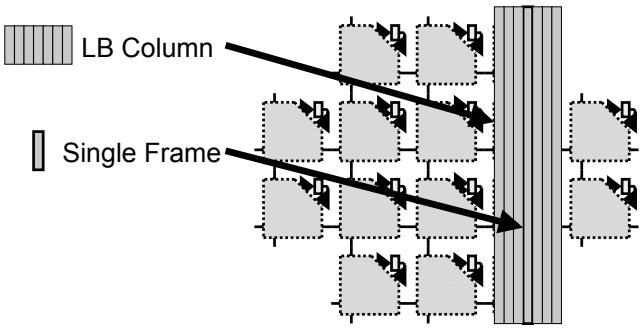
Jigsaw Puzzle Analogy

- FPGA composed of regular, identical tiles
  - Like pieces of a puzzle
    - Very few different tile types (4 in Virtex)



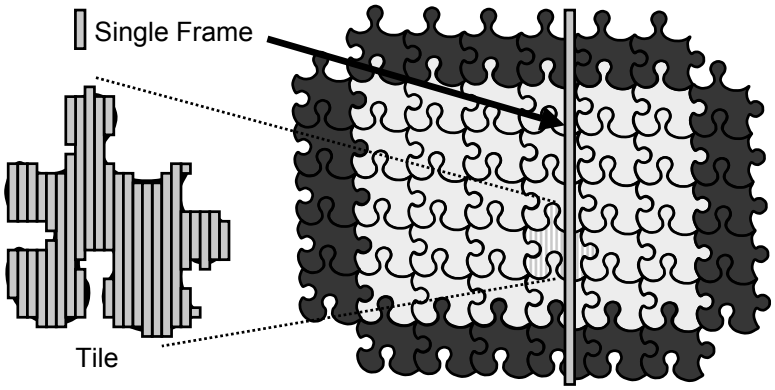
Configuration Data (1)

- Frame = smallest configuration unit [Xilinx 03]
  - 1 bit wide, spans height of FPGA
  - Contains some config. data for many blocks
    - 48 frames per LB column (48 bits wide)

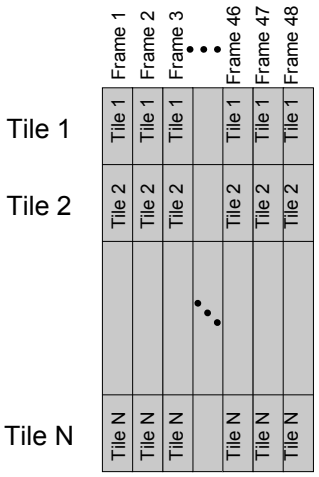


Configuration Data (2)

- Tile can't be independently configured
  - Config. data spread over multiple frames



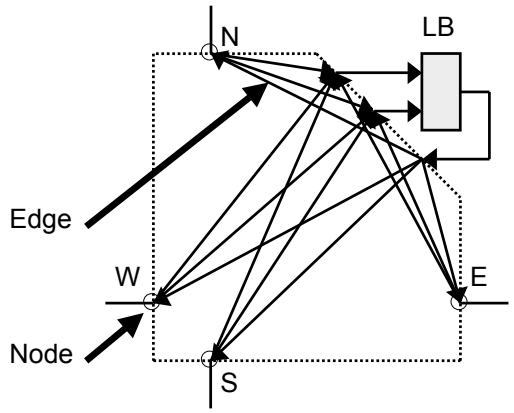
Configuration Data (3)



LB Column Configuration Data

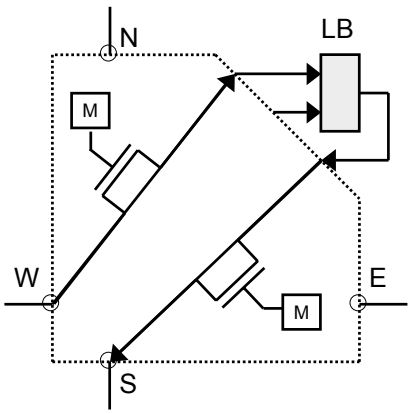
Switch Matrix Directed Graph

- Connects wires
- Composed of edges and nodes



Switch Matrix PIP Implementation

- Edge = PIP, node = wire
- Each PIP controlled by SRAM cell



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Motivation (1)

- FPGA manufacturing testing
  - Logic is easy
  - Routing resources are difficult
    - Hundreds of SMs, thousands of PIPs per SM
      - Millions of PIPs
      - Billions of possible configurations

Motivation (2)

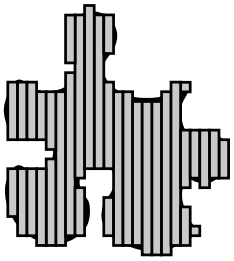
- Test time
  - Dominated by configuring (80%), not testing
    - Configuration time ~ seconds [Xilinx 02]
    - Test pattern application time ~ milliseconds
    - Total test time ~ minutes [Toutounchi 03]

Motivation (3)

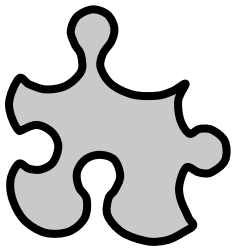
- Storage space
  - Dominated by config. data, not test vectors
    - Hundreds of configs. needed to test routing
- Test configuration generation
  - Tedious, generated manually [Toutounchi 02]
    - Maximize use of wires and PIP
    - Minimize total number of configurations

Architecture Modification

- Configure tiles, not frames
  - Smallest unit of configuration = tile
    - Modify configuration data addressing logic
    - Modify configuration data wiring



Many frames

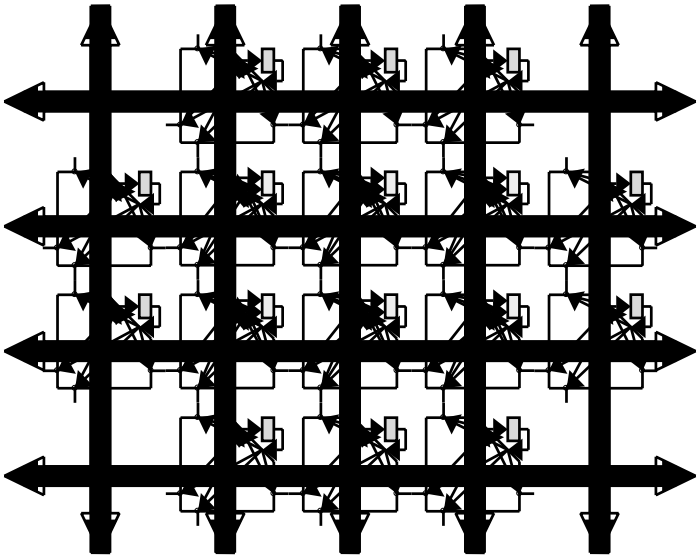


Single ‘frame’

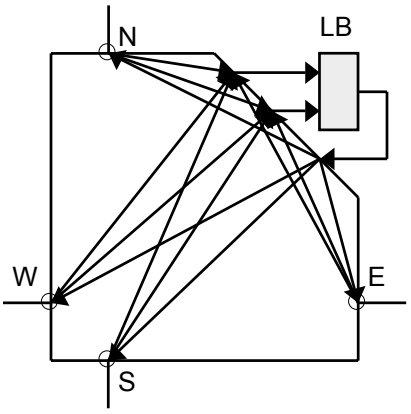
General Testing Methodology

- Iterate
  - Configure FPGA into ILAs
    - Turn on only certain PIPs in SMs
    - Each ILA is identical
      - All like tiles configured identically
      - All tiles configured simultaneously
  - Apply test input
  - Observe response

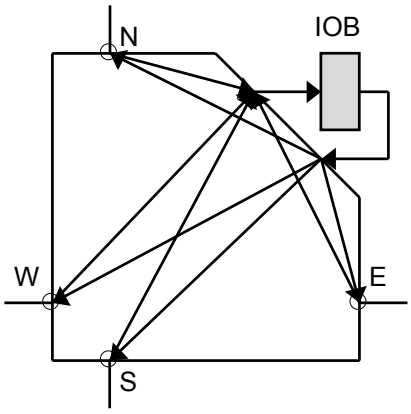
Example ILA Directions



Example Tiles

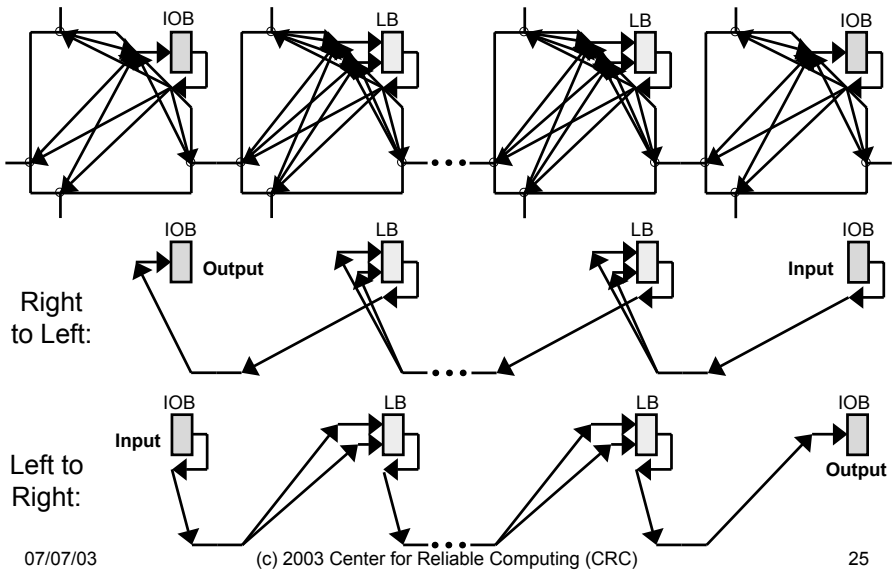


Logic Block Tile

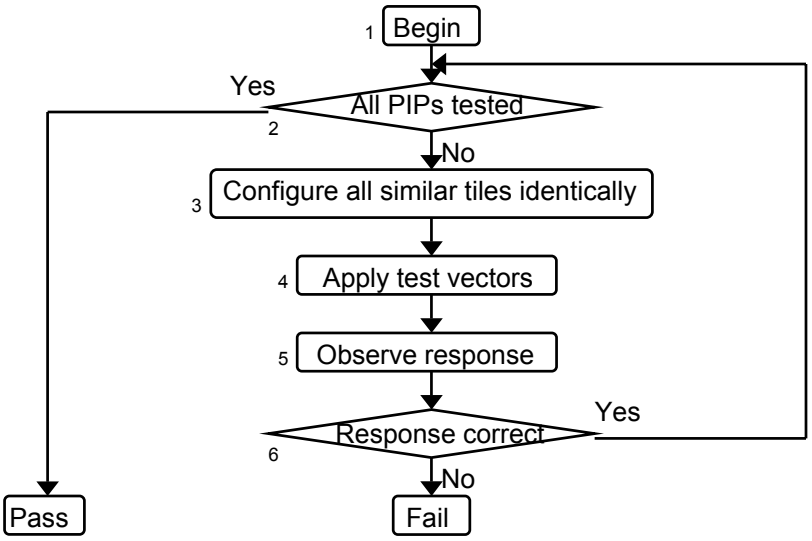


Input/Output Block Tile

Example Horizontal ILAs



Testing Flow

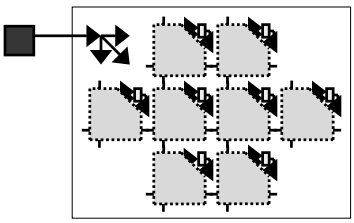


Architecture Modification Benefits

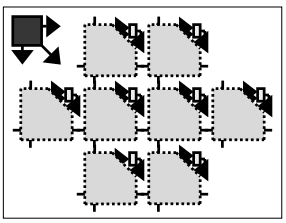
- Given FPGA with *N* tiles
  - Configuration data storage
    - Reduced to ~ 1/*N* of original
    - Config. data stored once per tile type
  - Total test time
    - Reduced to ~ 1/*N* of original
    - Configure tiles simultaneously, externally
  - Configuration generation
    - Reduced to single tile, not whole FPGA

BIST Enhancement

- Configure internally, not externally
  - Add BIST hardware (state machine)
    - Internally configures tiles
    - One state machine per tile type, 4 total
      - LB, IOB, Block RAM, Multiplier tiles



External Configuration



Internal Configuration

BIST Enhancement Benefits

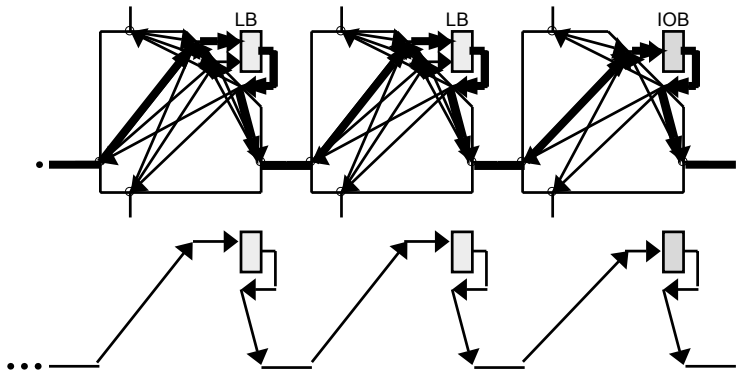
- Given FPGA with *N* tiles:
  - Configuration data storage
    - Eliminated
    - Configs. generated by BIST hardware
  - Total test time
    - Reduced to < 1/*N* of original
    - Configure tiles simultaneously, internally
  - Configuration Generation
    - Reduced to single tile, not whole FPGA

Configuration Generation (1)

- Performed for each PIP (ILA) direction

1. Choose output PIP from {untested}
   PIP connected to output of block
2. Trace output to next element (SM or block)
3. Choose input PIP from {untested}
   PIP connected to input of block
   If ø, choose regular PIP, goto 2.
4. {tested} = output PIP + input PIP
5. {untested} = {untested} – {tested}
6. Config. complete, iterate until {untested} = ø

Configuration Generation (2)



1. Choose egress PIP
2. Trace output to next element
3. Choose ingress PIP

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Configuration Generation (1)

- Group PIPs based on wires
  - Type (length)
    - Fast, direct, double, hex, long
  - Direction
    - Vertical (left, right)
    - Horizontal (up, down)
    - Diagonal (up-left, up-right, down-left, etc...)
- Configure ILAs based on PIPs
  - Diagonal not restricted to 45º path

Configuration Generation (2)

- Multiple blocks per SM
  - PIPs associated to different blocks
    - Test with same ILA configuration
      - Single ILA incorporates multiple blocks

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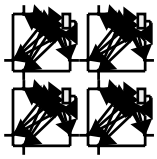
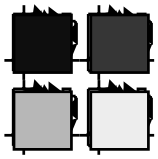
Configuration Data Shifting (1)

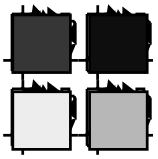
- Shift config. of Unit Element (UE) [Doumar 99]
  - Unit element = switch matrix + logic block
- Each UE has unique configuration



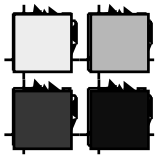
2x2 FPGA



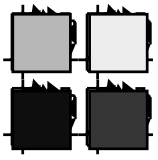
Config 1 (original)



Config 2 (shift right)



Config 3 (shift down)



Config 4 (shift right)

Configuration Data Shifting (2)

- Assumptions
  - Config. data organized as a shift chain
    - Divides chain via muxes
    - Inputs to muxes from adjacent UE
  - # UEs > # different configurations
- Ambiguities
  - Interconnection of UEs
  - Connections of UEs to external pins
  - Test coverage of all PIPs

Automatic Configuration Generation (1)

- Group PIPs [Tahoori 03]
  - Horizontal, vertical, left diag., right diag.
- Generate Iterative Logic Arrays (ILAs)
  - Direction limited to row, column, or diagonal
  - Maximum flow graph algorithm
- Tested via BIST (configured logic blocks)
  - Test pattern generator
  - Output response analyzer

Automatic Configuration Generation (2)

- To test all PIPs and wires in Virtex
  - Only 8 configurations needed
- Assumptions
  - Over-simplified model of switch matrix
    - PIPs connect wires of different directions
      - ILA direction limitation invalid

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Future Work

- Configuration generation
  - Automate
    - PIP covering problem
    - Graph traversal algorithm
    - 3000+ PIP connections per SM for Virtex-II
    - 100+ wire connections per SM for Virtex-II
- BIST hardware
  - Translate configurations into state machine
  - Determine area overhead

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Conclusion

- Modify configuration architecture
  - FPGA layout very regular
    - Tile = smallest unit of configuration
- Enhance configuration architecture
  - Dedicated BIST hardware
    - Internally configure device
- Total test time reduced
- Configuration data storage reduced
- Configuration generation simplified

References

[Doumar 99] Doumar, A. and Ito, H. “Testing the Logic Cells and Interconnect Recources for FPGAs,” Eighth Asian Test Symp., pp. 369-374, 1999.

[Tahoori 03] Tahoori, M. and Mitra, S. “Automatic Configuration Generation for FPGA Interconnect Testing,” Proc. VLSI Test Symp., pp. 134,139, 2003.

[Toutounchi 02] Toutounchi, S. and Lai, A. “FPGA Test and Coverage,” Proc. Int’l Test Conf., pp 599-607, 2002.

[Toutounchi 03] Toutounchi, S. Personal Correspondence, 2003.

[Xilinx 02] Xilinx, Inc. “The Programmable Logic Data Book,” 2002.

[Xilinx 03] Xilinx, Inc. “Virtex Series Configuration Architecture User’s Guide,” 2003.