Center for
Reliable
Computing

FPGA Interconnect Bridging Fault Detection and Location via Differential IDDQ

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Outline

- Introduction
- Differential IDDQ
- Bridging Fault Location
- Conclusion

Field-programmable Gate Array

- Configurable integrated circuit
  - Programmable logic
    - Look-up Tables (LUTs)
      - Boolean function truth table
    - Bistables
      - Flip-flop or latch
  - Programmable interconnection network
    - Programmable Interconnect Points (PIPs)
      - 80% of die area

IDDQ

- Steady-state device current
  - Detect bridging fault
    - Fault current
- Smaller process dimensions
  - More transistors
    - Larger IDDQ
  - Constant fault current
    - Difficult to detect
      - Process variation

Differential IDDQ

- Difference in pair of IDDQ measurements
  - Cancel device leakage current
    - Easier to observe fault current
- Not completely possible for ASIC
  - Fixed logic and inversion
- Possible for FPGA
  - Configurable logic
    - LUT Boolean function, F
    - Bistable initial condition, init

Differential IDDQ for FPGA

- Measure reference current, $IDDQ_{ref}$
  - All interconnects logic-1
    - Device leakage only
- Measure total current, $IDDQ_{tot}$
  - Subset interconnects logic-0
    - Device leakage + fault current
- Calculate signature current, $IDDQ_{sig}$
  - $IDDQ_{tot} – IDDQ_{ref}$
    - Compare to threshold

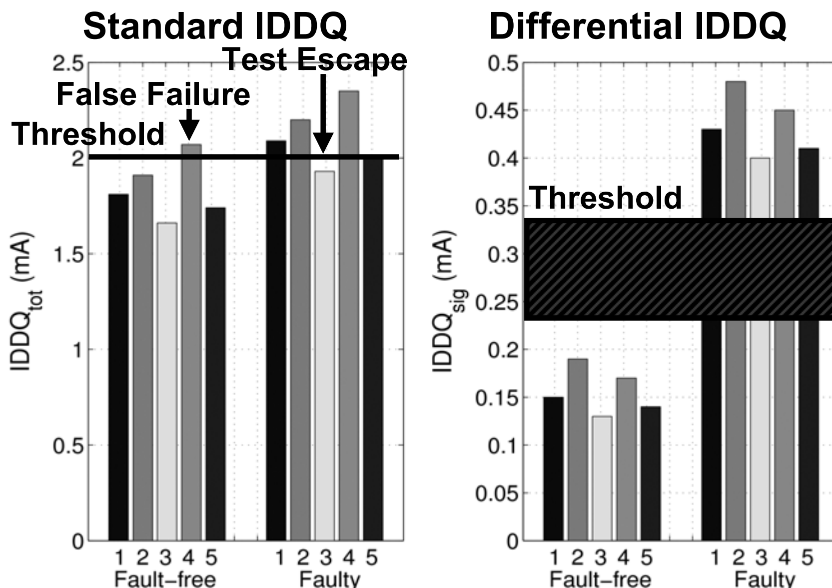
Fault Detection Experiment

- 5 Xilinx 90 nm Spartan-3 XC3S50
  - Emulate bridging fault
    - Activate unused PIP (0.5 – 1 kΩ bridge)
- Detectability ratio
  - Fault current ÷ current compared to threshold
    - Standard: $d_s = IDDQ_{fault} \div IDDQ_{tot}$
    - Differential: $d_d = IDDQ_{fault} \div IDDQ_{sig}$
- Improvement ratio
  - $i = d_d \div d_s = IDDQ_{tot} \div IDDQ_{sig}$

Fault Detection Results

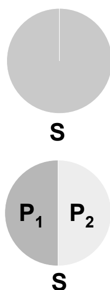
Dev.	IDDQ (mA)						Detectability		Imp.
	ref	Fault-free		Faulty		fault	d_s	d_d	i
		tot	sig	tot	sig		(std.)	(diff.)	
1	1.66	1.81	0.15	2.09	0.43	0.28	0.13	0.65	5.0
2	1.72	1.91	0.19	2.20	0.48	0.29	0.13	0.60	4.6
3	1.53	1.66	0.13	1.93	0.40	0.27	0.14	0.68	4.9
4	1.90	2.07	0.17	2.35	0.45	0.28	0.12	0.62	5.2
5	1.60	1.74	0.14	2.01	0.41	0.27	0.13	0.66	5.1

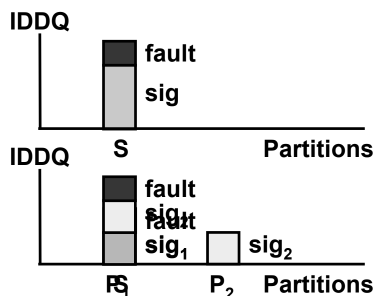
Threshold Comparison



Resource Partitioning

- Further increase fault current detectability
  - Divide nets of FPGA into partitions
  - Test each partition independently
- Locate bridging fault

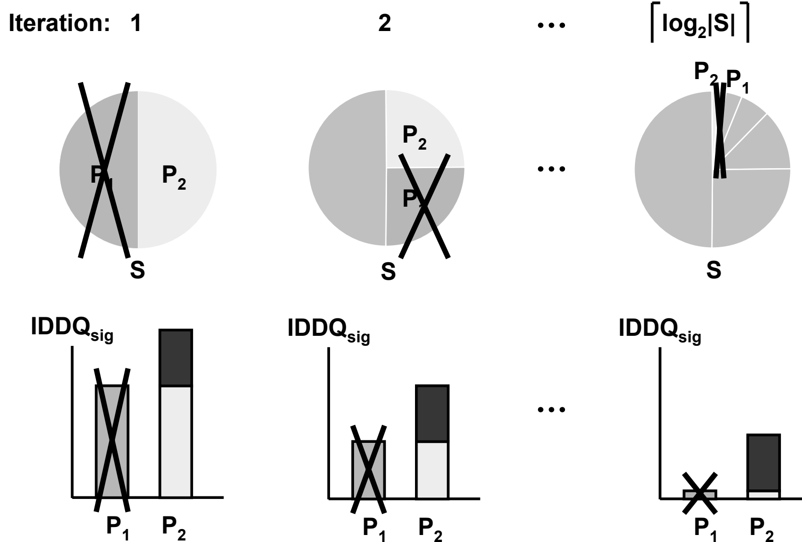




Bridging Fault Location

- Locate bridged net
  - Partition nets of FPGA
  - Test each partition independently
  - Eliminate nets of fault-free partition
  - Iterate
- Fully automated
  - Only configuration and measurement
- Running time logarithmic in |S|
  - $\lceil \log_2 |S| \rceil$ iterations (2 partitions per iteration)

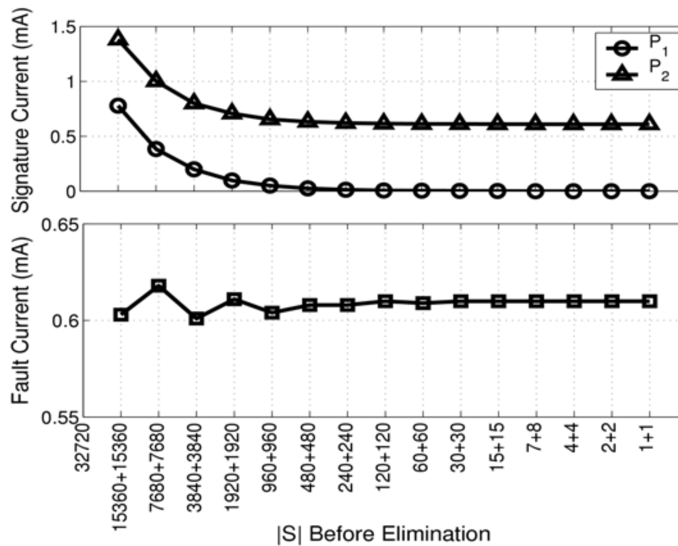
Fault Location Example



Fault Location Experiment

- Xilinx 90 nm Spartan-3 XC3S1000
  - Emulate bridging fault
    - Activate unused PIP (0.5 – 1 kΩ bridge)
- Manufacturing test configuration
  - Initially |S| = 30720 nets
    - 15 iterations (2 partitions per iteration)
      - $15 = \lceil \log_2 30720 \rceil$
    - 31 configurations and IDDQ measurements
      - $31 = 1\ IDDQ_{ref} + 2\ IDDQ_{tot}$ per iteration

Fault Location Results



Conclusion

- Differential IDDQ
  - FPGA configurability
  - 5x or greater improvement
    - Fault current detectability
  - Used in Xilinx EasyPath
- Fault location
  - Iterative partitioning and elimination
    - Logarithmic running time
    - Fully automated