Detecting Delay Flaws by Very-Low-Voltage Testing

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Purpose
- Detect Weak CMOS ICs at Low Cost
- Provide an Alternative to Burn-in
- Provide an Alternative to IDDQ

Outline
- Introduction
- Timing Defects
  - Causes
  - Failure modes
- CMOS Propagation Delay $T_d$
  - Voltage dependence
  - $T_d$ change rate
- Choosing Supply Voltage $V_{dd}$
  - Delay flaws
  - Conclusions

Introduction
- Delay Flaws
  - Excess delay in short path
  - Intermittent, early-life failures
- Previous Work
  - Supply voltage 2V to 2.5V for VLV testing
  - Test speed

Timing Defect Causes
1. Transmission Gate Opens
2. Threshold Voltage Shifts
3. Diminished-Drive
4. Defective Buffers
5. Gate Oxide Shorts
6. Metal Shorts
7. High-Resistance Interconnects
8. Via Defects
9. Tunneling Opens

Timing Failure Modes
1. Transmission Gate Opens
   - NMOS or PMOS transistor cannot pass signals
   - Degraded output signals
     - Next gates weakly driven, slower
2. Threshold Voltage Shifts
   - Smaller transconductance, driving strength
   - NMOS transistors bigger effects
     - Increased gate delays, slow-to-fall signals
### Timing Failure Modes

#### Diminished-Drive
- High-drive gates drive long wires, large fanout
- Redundant components cannot pass signals
- Increased gate delays, slow-to-rise, slow-to-fall

#### Defective Buffers
- Internal shorts
  - Degraded signals, high leakage,
  longer gate delays, longer interconnect delays
- Open faults
  - Cannot pass signals, stuck-open

#### Gate Oxide Shorts and Metal Shorts
- Degraded signals, increased leakage

#### High Resistance Interconnects
- Increased RC delays, slow-to-change along interconnects

#### Via Defects
- High resistance wires, opens, or shorts
- Increased RC delays, slow-to-change, stuck-open, or high leakage

#### Tunneling Opens
- Open interconnect
- No capacitive coupling between two ends
- Tunneling currents across opens
  - Pass signals at low frequency,
    fail at high frequency
- Gross delay faults
- Delay fault testing effective

#### VLV Testing Effective
- Degraded signals - 1, 4, 5, 6, 8
- Diminished-drive gates - 2, 3

#### VLV Testing Not Effective for High Resistance Interconnects
- RC delay does not change at low voltage
- Percentage of delay due to gates increases at low voltage
- Use delay fault testing at normal voltage

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CMOS Propagation Delay $T_d$
- Voltage Dependence
- Smaller driving capability at low voltage

\[ T_d = \frac{C_L \times V_{dd}}{\mu \cdot C_{ox} (W/L) (V_{dd} - V_i)^2} = K \frac{V_{dd}}{(V_{dd} - V_i)^2} \]

CMOS $T_d$ - Degraded Signals
- Input Signal is Degraded to $V_{dd}/a$
  - $T_{wd}$: $T_d$ of weakly driven gate
    \[ T_{wd}(V_{dd}) = K \frac{V_{dd}}{(V_{dd}/a - V_i)^2} = a \times T_d(V_{dd}/a) \]
  - $T_d(V_{dd}/a) = K \frac{V_{dd}}{(V_{dd}/a - V_i)^2}$
- Similar Relationship for Threshold Voltage Shifts
  - $T_{sh}$: $T_d$ of threshold-voltage-shifted gates
    \[ T_{sh}(V_{dd}) = a_s \times T_d(V_{dd}/a_s) \]

CMOS $T_d$ - Delay Ratios
- Weakly-Driven and Fault-Free Gates
  - $T_{wd}(V_{dd}) / T_d(V_{dd})$
  - Increase significantly at low voltage

<table>
<thead>
<tr>
<th>$V_{dd}$</th>
<th>$V_{dd}/V_{in}$</th>
<th>$T_{wd}(V_{dd})$</th>
<th>$T_d(V_{dd})$</th>
<th>$V_{dd}/V_{in}$ Delay Ratio</th>
<th>$T_{wd}(V_{dd})$ Delay Ratio</th>
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<tbody>
<tr>
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$T_d$ Change Rate
- $T_d(V_{dd} - \Delta V_{dd}) / T_d(V_{dd})$, $\Delta V_{dd} = 0.2V$

V_{dd} for VLV Testing
- $T_d$ Change Rate Significant
  - Between $2V_{i}$ and $2.5V_{i}$
  - Similar to previous conclusion [Chang 96]
- Use Several Delay Flaws to Verify This Statement
  - Transmission gate opens
  - Threshold voltage shifts
  - Diminished-drive

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Transmission Gate Opens

Simulated Circuits
- Full adder cell built by pass-gate logic
- Transmission gate opens in T1 and T3

Simulation Setup
Incorporate faults into CSA11 and CSA22 cell

Threshold Voltage Shifts

Simulated Circuits
- Global Threshold Voltage Shifts

Diminished-Drive

Simulated Circuit
- $T_d$ measured from $V_a$ to $V_{out}$

Supply Voltage $V_{dd} / \frac{V_{th}}{V_{tn}}$ Path Delay Ratio $T_d$ (faulty) / $T_d$ (fault-free)

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>$V_{dd} / \frac{V_{th}}{V_{tn}}$</th>
<th>CSA22 T1 NMOS Open</th>
<th>CSA22 T1 PMOS Open</th>
<th>CSA22 T3 NMOS Open</th>
<th>CSA22 T3 PMOS Open</th>
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</table>

* stuck-open

Supply Voltage $V_{dd} / \frac{V_{th}}{V_{tn}}$ Delay Ratio $T_d$ (faulty) / $T_d$ (fault-free)

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>$V_{dd} / \frac{V_{th}}{V_{tn}}$</th>
<th>$\Delta V_t = 0.2V$</th>
<th>$\Delta V_t = 0.3V$</th>
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Supply Voltage $V_{dd} / \frac{V_{th}}{V_{tn}}$ Diminished-Drive

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>$V_{dd} / \frac{V_{th}}{V_{tn}}$</th>
<th>$\Delta V_t = 0.2V$</th>
<th>$\Delta V_t = 0.3V$</th>
<th>$\Delta V_t = 0.4V$</th>
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</table>
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## Summary

<table>
<thead>
<tr>
<th>Causes</th>
<th>Detected by</th>
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</thead>
<tbody>
<tr>
<td>Transmission gate opens</td>
<td>V D I</td>
</tr>
<tr>
<td>Threshold voltage shifts</td>
<td>V D I</td>
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<tr>
<td>Diminished-drive gates</td>
<td>V D I</td>
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<tr>
<td>Defective buffers</td>
<td>V D I</td>
</tr>
<tr>
<td>Gate oxide shorts</td>
<td>V D I</td>
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<tr>
<td>Metal shorts</td>
<td>V D I</td>
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<tr>
<td>High resistance interconnects</td>
<td>V D I</td>
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<td>Via defects</td>
<td>V D I</td>
</tr>
<tr>
<td>Tunneling opens</td>
<td>V D I</td>
</tr>
</tbody>
</table>

V: VLV testing  
D: delay fault testing  
I: IDDQ testing

## Test Speed

- Gate and Interconnect Delays Scale Differently as $V_{dd}$ is Reduced
  - All CMOS gate delays scale similarly when $V_{dd}$ is changed
  - Interconnect delays remain almost the same at different $V_{dd}$
- Must Characterize Speed-Voltage Relationship More Thoroughly
  - Shmoo plots
  - Test Speed No Worse Than 10 Times Slower

## Conclusions

- VLV Testing Can Detect
  - Transmission gate opens
  - Threshold voltage shifts
  - Diminished-drive
  - Gate oxide shorts
  - Metal shorts
- Supply Voltage $2V_{i}$ to $2.5V_{i}$ for VLV Testing

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