Testing for Resistive Opens in FPGA

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Outline
- Introduction
  ◆ Resistive open in ASIC
  ◆ FPGA
- New Technique
- Simulation Results
- Summary

Resistive Open
- Imperfect connection between two nodes
  ◆ Defect resistance
- Causes:
  ◆ Bad Contact
  ◆ Bad Via
  ◆ Bad Transistor
  ◆ Thin Wire

Modeling
- Delay of defective chain
  \[ Delay = [R_n(V_{DD}) + R_{o/T}] \cdot C \]
- \( R_{o/T}(V_{DD}) \): Transistor turn-on resistance
  ◆ Function of \( V_{DD} \)

Terminology
- Delay Delta [Li ITC01]
  ◆ Defective Circuit Delay – Good Circuit Delay
- Delay Ratio
  \[ \frac{\text{Defective Circuit Delay}}{\text{Good Circuit Delay}} \]
- Testing for resistive open
  ◆ Making delay ratio bigger

Issues in ASIC
- Fixed circuit
- Controllable Parameters
  ◆ Test Voltage
  ◆ Test Temperature
  ◆ < 10% change [Li, ITC01]
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Switch Matrix

Issues in FPGA

- Circuit is NOT fixed
  - Reprogrammable
  - Lots of available unused routing resources
    - Even with 100% logic utilization
- Controllable parameters
  - Test voltage
  - Test temperature
  - Load capacitance

Modeling in FPGA

- Simple routing path
  - Consist of PIP and logic blocks

SPICE Simulation

- TSMC 0.18 technology
- Different voltages and defect values
  - Nominal: 2.5 V
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Voltage Effect on Delay

Delay vs Defect size

Delay Delta

Delay Delta

Delay Ratio

Delay Ratio

Conclusion

- Higher voltage higher delay ratio
  - Better detectability
  - At most 10% improvement
  - Still need at speed test

New Technique

- Change load capacitance
- By activating additional paths
- Increase delay ratio significantly

Circuit Model

- Adding one additional fanout
- Turning on one more PIP
- Maximum number of fanouts
- Number of PIPs connected to A
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Delay with Additional Fanouts

Delay with Additional Branches

Delay Delta

Delay Delta with Additional Branches

Delay Ratio

Delay Ratio with Additional Branches

SPICE Simulation Results

- Consider only nominal voltage
- Significant increase in delay ratio
  - Almost twice with one additional fanout
  - Proportional with number of fanouts
- Better results for larger defects
- No need to at-speed test

More Improvement

- Consider line segments in additional fanouts
- When PIPs are not buffered
  - Contributed to load capacitance

Circuit Model

- Wire modeled as RC network
  - Lumped model

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SPICE Simulation Setup
- TSMS 0.18 μm technology
- Two kinds of wires
  - Short Wire (100 μm)
    - Single lines
    - $R_w = 10 \, \Omega$, $C_w = 43 \, \text{fF}$
  - Long wire (1.4 mm)
    - Hex and long lines
    - $R_w = 140 \, \Omega$, $C_w = 615 \, \text{fF}$

Delay with Wires
- Graph showing delay with wires for different branch conditions:
  - No Branch
  - 1 Branch
  - 2 Branches
  - Short Wire
  - Long Wire

Delay Delta
- Graph showing delay delta for different conditions:
  - Graph axes: Defect Value (K ohm) vs. Delay Delta (ns)

Delay Ratio
- Graph showing delay ratio for different conditions:
  - Graph axes: Defect Value (K ohm) vs. Delay Ratio

Simulation Results
- Promising
- One additional PIP + short wire
  - Better than two additional PIPs
- More effective with longer wires
- Delay ratio several times increased
- Detect fault at lower tester speed
- Avoid at-speed test

Summary
- Resistive opens in FPGAs
  - Increase load capacitance
  - Additional fanouts
  - Programmability
  - Abundant unused PIPs
- New technique
  - Add more fanouts
  - For buffered PIPs
  - Use line segments in fanouts
  - For unbufferd PIPs
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Summary (con’t)
- Simulation results
- Multiple times improvement
- Scalable
- Avoid at-speed test